64000

HP 64000 Logic Development System

Model 64501A Positive PROM Programmer

HEWLETT PACKARD

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SAFETY SYMBOLS

General Definitions of Safety Symbols Used on Equipment or in Manuals.

Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).

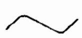
 **OR** 

Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.

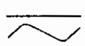
 **OR** 

Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).

Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE:

The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

HEWLETT-PACKARD

SERVICE MANUAL

MODEL 64501A

POSITIVE PROM PROGRAMMER

REPAIR NUMBERS

This Manual applies directly to Models with Repair Numbers prefixed 24XXA. The Performance Verification in this manual is supported by software revcoded 2406 or later. Any other PROM Programmer software is supported by the 64500-90910 Manual ONLY. Section VII is the Backdating section for Models with Repair Numbers prefixed 2239A or 1924A that have a 64501-66502 board installed. Models with repair numbers prefixed 1924A that have a 64501-66501 board installed are serviceable with the 64500-90910 Manual ONLY.

Manual Part Number 64500-90911

Printed: January 1984

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Each new edition of this manual incorporates all material updated since the previous edition. Manual Updates are issued between editions, instructing you to add, replace, or remove pages in the current edition.

The print date changes only when each new edition is published. Minor corrections or additions may be made as the manual is reprinted between editions. Vertical bars in a page margin indicate the location of reprint corrections.

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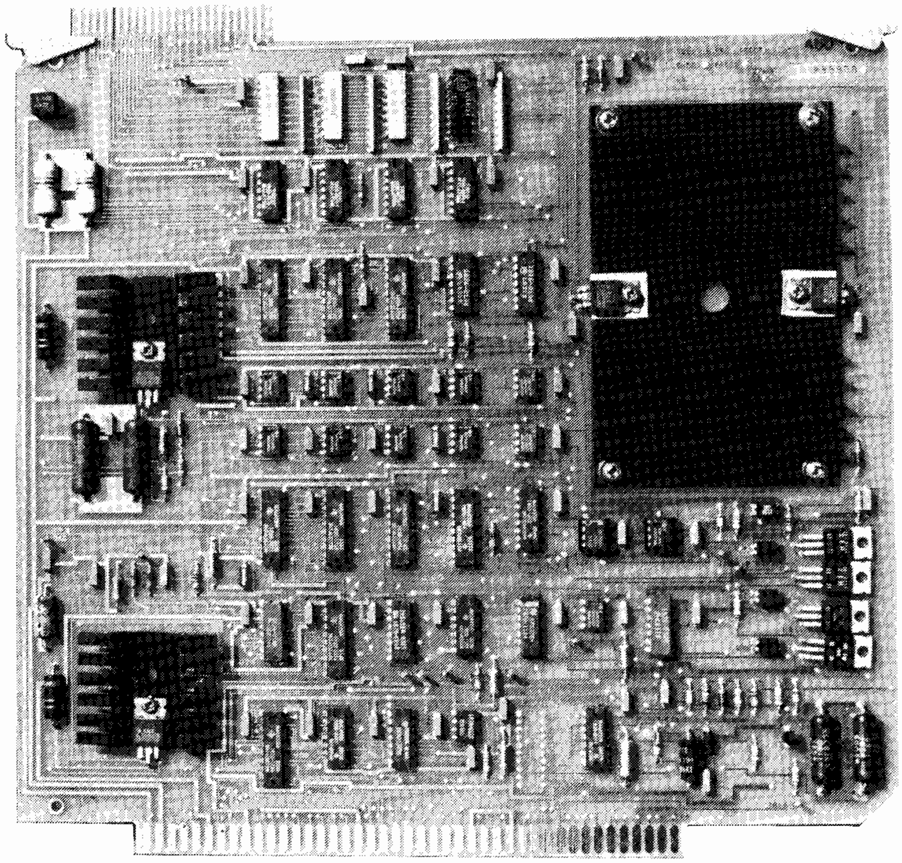


Model 64501A PROM Programmer Control Board

Interface Cable

Figure 1-1. Model 64501A Prom Programmer Contents

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Hewlett-Packard Model 64501A PROM Programmer Control board. Operating instructions are provided in a separate Operating Manual supplied with this instrument. It should be kept with the instrument for use by the operator.

1-3. INSTRUMENTS COVERED BY THIS MANUAL.

1-4. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last four are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-5. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument has been modified from those described in this manual. The manual for this modified instrument is accomplished by a Manual Change supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-6. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Change supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page.

1-7. For information concerning a repair number prefix that is not listed on the title page or in the Manual Change supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-8. DESCRIPTION.

1-9. The Hewlett-Packard Model 64500S Positive PROM Programmer is designed to program a wide variety of positive PROMs and EPROMs.

1-10. The Model 64500S consists of one Model 64501A Positive PROM Programmer Control board and one or more programmer modules. One Model 64502A Programmer Module is supplied with every 64500S. Other programmer modules must be ordered separately by model number, or by option as part of the Model 64500S.

1-11. Throughout this manual the Positive PROM Programmer will be referred to as the Model 64501A. It is the same as the Model 64500S except that the 64500S will have options included. The options are the programmer modules, i.e., Model 64502A, 64503A, 64504A, etc. The service information for the programer modules is covered in the Service Manual for that module.

1-12. The PROM Programmer board may be ordered as Model 64501A. If the board is being ordered for replacement purposes, use the ten digit part number from the material list. The older 64500S Prom Programmer subsystem may have contained a 64501A Prom Control board that was serial prefixed 1924A. These boards are supported by the 64500-90910 Service Manual ONLY.

1-13. The Model 64502A is used for Positive PROM Programmer Performance Verification tests, and programming Intel's 2716 and 2758, Texas Instrument's TMS2516, and TMS2532 programmable ROMs.

1-14. Pulse widths and sequences for the PROM being programmed are determined by the software.

1-15. Voltage levels, current levels, and rise or fall times are determined by the specific programmer hardware modules.

1-16. The Model 64500S performs the functions of reading, writing, and verifying of programmable memories.

SECTION II

INSTALLATION AND REMOVAL

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64502A. Included are initial inspection procedures and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically. The electrical Procedures for checking Performance Verification are given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify the nearest Hewlett-Packard Sales/Service office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Sales/Service Office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP's option without waiting for claim settlement.

2-5. INSTALLATION PROCEDURE.

2-6. When the Positive PROM Programmer is installed in the Mainframe, it should be positioned in the front most unused connector. This is typically the fourth or fifth connector from the front of the Mainframe. The Input/Output Controller, Display Controller, and the CPU boards occupy the first three connectors respectively. The Floppy or Tape Controller board occupies the fourth connector when installed.

NOTE

The Model 64501A Positive PROM Programmer and programmer modules must be installed and removed with the mainframe's power turned off.

2-7. PROM PROGRAMMER CABLE.

2-8. A 50 conductor ribbon cable, W1, connects the PROM Programmer to the programmer module. The end of the cable with the single connector is connected to the top left corner of the PROM Programmer with the cable towards the front of the mainframe. The cable should be routed across the top of the card cage and down behind the front panel. The two connectors should be visible in the opening for the programmer module. Depending on the module being used, it can have one or two PC boards. If it has only one board, use the connector nearest the end of the cable. The PC boards and cable connectors are keyed so that they fit together only one way.

SECTION III

OPERATION

3-1. The operation of the PROM Programmer is a function of the system software. Complete operation from the keyboard of the system is beyond the scope of the Service Manual. Please refer to the Operator's Manual for the procedures.

CAUTION

The proper operation of the positive PROM programmer requires that a PROM be inserted ONLY AFTER the PROM programmer software module is called and that the PROM be REMOVED before the PROM programmer software module is exited.

NOTE

The PROM software module is called by pressing the [prom_prog] softkey, then the RETURN key. To exit the PROM programmer software module, press the [end] softkey, then the RETURN key

SECTION IV

PERFORMANCE VERIFICATION AND TROUBLESHOOTING

4-1. INTRODUCTION.

4-2. The performance verification tests verify to approximately an 85% confidence level that the 64501A board is operational. With the addition of the Supply Adjust Test (which consists of the DAC output, the +10 volt VP3, and the VP3 Overload Detection Tests), the confidence level can be raised to approximately 98%. The Supply Adjust Test should only be performed by qualified Service Personnel.

4-3. There are five performance verification tests that verify if the PROM Programmer Control board and 64502A Module are operating properly. These tests are: The Address-ID test, the Data test, the Supplies test, the Failsafe test, and the Supply Adjust test. Each test will be explained in this section.

4-4. The Address-ID, Data, and the Supplies test all have signature analysis associated with them. If the ID for the Prom Programmer is not read correctly, then the ID test will automatically be entered. It too has a signature analysis loop for troubleshooting (see table 4-1).

Table 4-1. Available Signature Analysis Loops

Loop A	-	Run the "Address-ID" Performance Verification Test
Loop B	-	Run the "Data" Performance Verification Test
Loop C	-	Run the "Supplies" Performance Verification Test
Loop D	-	Can only be stimulated when an ID failure occurs

*** When taking signatures, make sure the [start] softkey is used to ***
*** initiate signature analysis stimulus and not the [cycle] softkey. ***

4-5. EQUIPMENT REQUIRED.

4-6. A Model 5005A/B Signature Analyzer, an Oscilloscope, and a ET19783 Extender board are needed to troubleshoot the 64501A board.

4-7. The HP Model 64502A Programmer Module must be installed when running the PROM Programmer Control board Performance Verification. See the 64502A Service Manual for the installation procedure.

NOTE

The Model 64502A PROM Module is the only module that can be used to run Performance Verification on the 64501A PROM Programmer Control board. Other PROM Programmer Modules have different ID's than the 64502A and will not enable the performance verification. Since the wrong ID would be called up, the system software will treat it as an ID failure and automatically enter into the ID Test.

4-8. If a problem does occur, refer to the Performance Verification theory for an understanding of its operation. This will help in troubleshooting the 64501A PROM Programmer Control board and the 64502A Prom Module.

4-9. RUNNING THE PERFORMANCE VERIFICATION.

a. From the Keyboard call up the PROM Performance Verification. This is done by pressing the [opt_test] softkey followed by the RETURN key. A table will be displayed indicating the location of the option boards in the card cage of the mainframe. Press the number corresponding to the slot number which the PROM Controller board occupies followed by the RETURN key.

b. Press the [cycle] softkey to run the Performance Verification on the first four tests. The fifth test (Supply Adjust) is a measurement and adjustment test. An oscilloscope/voltmeter is required for this test. Note the Pass/Fail response. If a failure occurs then troubleshoot that failure with signature analysis.

4-10. PERFORMANCE VERIFICATION THEORY.

4-11. The Prom Programmer Control board circuitry is effectively tested by the performance verification software to approximately an 85% confidence level. If one of the performance verification tests does not pass, set up and use signature analysis to troubleshoot the failure. Only qualified Service Personnel should troubleshoot a failure.

```
                    Prom Programmer Performance Verification

 Prom Programmer in card slot #   1

  Test                                                 # Fail   # Test

 Address-ID                                               0        0

 Data                                                     0        0

 Supplies                                                 0        0

 Failsafe                                                 0        0

 Supply Adjust                                           N/A       0



STATUS: Awaiting test selection _______________________________ 14:18

 -

 ___end___ __cycle__ next_test __dsp_test ________ ________ ________ __print__
```

Figure 4-1. Prom Programmer Performance Verification Display

4-12. PRELIMINARY ID TEST. The ID Test is only entered when the 64502A Prom Prom Programmer Module's ID is not recognized or another module is used instead. It can be manually entered by grounding U6A pin 12 before and while entering performance verification to access the Preliminary ID Test test and Signature Analysis Loop D stimulus. Performance verification can ONLY be run on the 64501A Prom Programmer Control board when the 64502A module is attached. If the correct ID code (01H) is not read from the module, then the main selection of tests is not displayed. Instead, a limited ID test is offered where the address latches are set up to a specific pattern and a certain ID code is expected to be read according to the following pairs:

Table 4-2. ID Test Code

HEX ADDRESS	HEX DATA
C000	19
C001	01
C002	03
C004	05
C008	07
C010	09
C020	0B
C040	0D
C080	0F
D000	39
E000	59
F000	79

```
                    Prom Programmer Performance Verification

  Prom Programmer in card slot #   1

   Test                                                          # Fail   # Test

  Socket ID                                                          0        0

  64502A prom module ID not detected-only ID test may be run



  STATUS: Awaiting option_test command ________________________________ 14:18


     end              dsp_test                                     print
```

Figure 4-2. ID Test Display

4-13. The ID Test exercises the following components on the board:

Outward Transfer Path:		Inward Transfer Path:	
Address Block:		ID Block:	
U3A, U3B	Latch	U3C	Latch
U2A, U2B	Diode packs	U2C	Diode Pack
RP1, RP2	Resistor Packs	RP3	Resistor Pack
UR1A, UR1B	Resistor Packs	UR1C	Resistor Pack

4-14. The ID Test displays Pass/Fail information on the 7 bits of data from the ID Buffer. If any bit fails, then its bit position is assigned a "1" value. A "0" value means it has passed the test. The least significant bit refers to the data path which ends at U3C-18 and is sourced from VR4. The MSB refers to the data path of U3C-12. There is a combination of address lines, VP1, VP2, and VP3 which influence the upper 6 bits. If failures occur on U4E, U5E, U7F, VR3, or or VR4 this test could fail (only on some bits).

4-15. ADDRESS-ID TEST. The Address-ID Test outputs to the address latches and then reads from the ID lines in the same way that the ID Tests does, but it adds more pairs of data. The following is a list of the data pairs:

Table 4-3. Address Latch Data Pairs

HEX ADDRESS	HEX DATA
C000	19
C001	01
C002	03
C004	05
C008	07
C010	09
C020	0B
C040	0D
C080	0F
D000	39
E000	59
F000	79
8001	00
C100	11
C200	13
C400	15
C800	17
4000	0F

4-16. The Address-ID Test exercises the following components on the board:

Outward Transfer Path:

Address Block:

U3A, U3B	Latch
U2A, U2B	Diode Packs
RP1, RP2	Resistor Packs
UR1A, UR1B	Resistor Packs

Others:

U4E, U5E	Buffer
VR2, VR4	Adjustable Voltage Regulators

Inward Transfer Path:

ID Block:

U3C	Latch
U2C	Diode Pack (partial)
RP3	Resistor Pack
UR1C	Resistor Pack

4-17. The Address-ID Test gives Pass/Fail information on the 7 bits of data from the ID Buffer. If any bit fails, then its bit position is assigned a "1" value. A "0" value means it has passed the test. The least significant bit refers to the data path which ends at U3C-18 and is sourced from VR4. The MSB refers to the data path of U3C-12. There is a combination of address lines, VP1, VP2, and VP3 which influence the upper 6 bits. If a failure occurs on U7F this test could fail.

```
                    Prom Programmer Performance Verification
                                  Address-ID
  Prom Programmer in card slot #    1

   Test          results   (cumulative results)                 # Fail   # Test

  ID buffer       0000000   (0000000)                                0        0


  STATUS: Awaiting test selection ______________________________________ 14:18

  _

  ______ ______ ______ __start__ exit test ______ ______ __print__
```

Figure 4-3. Address-ID Test Display

4-18. DATA TEST. The Data Test outputs the data sequence 0000 thru 00FFH to the Prom Programmer data register and reads the data back.

```
                     Prom Programmer Performance Verification
                                      Data
  Prom Programmer in card slot #    1

   Test          results    (cumulative results)                 # Fail  # Test

  Data buffer    00000000   (00000000)                                0       0


  STATUS: Awaiting test selection ________________________________  14:18

  -

  ________ ________ ________ __start__ exit test ________ ________ __print__
```

Figure 4-4. Data Test Display

4-19. The Data Test exercises the following components on the board:

Outward Transfer Path:

Data Out Block:

U6B	Latch
U4A - U4D	Buffers
U5A - U5D	Buffers

Inward Transfer Path:

Data In Block:

U6C	Buffer
U2C, U2D	Diode Pack
U3D, U3E	Comparators
RP4	Resistor Pack
UR1D	Resistor Pack

4-20. The Data Test gives Pass/Fail information on the 8 bits of data from the Data Buffer. If any bit fails, then its bit position is assigned a "1" value. A "0" value means it has passed the test. The least significant bit refers to the data path which ends at U6C-18 and is sourced from U6B-3. The MSB refers to the data path of U6C-9 and U6B-18.

4-21. SUPPLIES TEST. The Supplies Test uses the ID lines to determine if the supplies are working during Hot Socket.

NOTE

> The Prom Programmer Control board controls power to the Prom module. HOT SOCKET refers to when power is applied to the Prom module. COLD SOCKET refers to when the power is turned OFF to the Prom module.

The following tests are repeated 10 times to give a better scope presentation:

a. Address register set to 3FFFH, VP3 set to 1.2 volts. Reads the ID bits. Test the ID result to see that VP1 was low.

b. Address register set to 7FFFH, VP3 still at 1.2 volts. Reads the ID bits. Test the ID result to see that VP1 was high.

c. Address register remains at 7FFFH, VP3 is set to its maximum voltage of 26.7 volts. Reads the ID bits. Test the ID result to see that VP3 was high, and that VP2 was low.

d. Address register remains at 7FFFH, VP3 is set to its minimum voltage of 1.2 volts. Reads the ID bits. Test the ID result to see that VP3 was low.

```
                   Prom Programmer Performance Verification
                                  Supplies
  Prom Programmer in card slot #   1

   Test          results    (cumulative results)               # Fail   # Test

  VP1 test       passed     (passed)                              0        0

  VP2 test       passed     (passed)

  VP3 test       passed     (passed)










  STATUS: Awaiting test selection ________________________________ 14:18

  -

  ________ ________ ________ __start__ exit test ________ ________ __print__
```

Figure 4-5. Supplies Test Display

4-22. The Supplies Test exercises the following components on the board:

Outward Transfer Path:

Address Block:

U3A, U3B, U8A	Latch
U2A, U2B	Diode Packs
RP1, RP2	Resistor Packs
UR1A, UR1B	Resistor Packs

DAC Block:

U8A	Latch
U7A	Digital to Analog Converter
U6G	Op Amp
VR2	Adjustable Voltage Regulators

Others:

VR3, VR4	Adjustable Voltage Regulators
U4E, U5E	Buffer
U7F	Buffer

Inward Transfer Path:

ID Block:

U3C	Buffer
U2C	Diode Pack (partials)
RP3	Resistor Pack
UR1C	Resistor Pack

4-23. The Supplies Test displays Pass/Fail information on the three controllable supplies called VP1, VP2, and VP3. If any controllable supply fails, then it is assigned a fail tag on the display. A pass tag means it has passed the test. If VP3 fails, check the DAC block. If VP2 fails, then check VR3, U7F, and U5E. If VP1 fails, then check VR4, U7F, and U4E.

4-24. FAILSAFE TEST. The Failsafe Test checks the failsafe timer to make sure it responds in the proper time frame and that it can be reset with software control. The following test sequence is used:

a. The address lines are set to 0, data lines set to 0, and VP3 set at 26.7 volts (maximum voltage).

b. The data and ID are read to make sure they are not the Failsafe values. Any results that are the Failsafe values are recorded by setting the Failsafe error flag on the display.

c. Wait 400 milliseconds. This is too short for the Failsafe to have expired.

d. The data and ID are read to make sure they are not the Failsafe values. Any results that are the Failsafe values are recorded by setting the Failsafe error flag on the display.

e. The Failsafe Timer is reset so that it will not expire for at least another 500 milliseconds.

f. Wait 400 milliseconds more. This is too short for the Failsafe to have expired since it was reset.

g. The data and ID are read to make sure they are not the Failsafe values. Any results that are the Failsafe values are recorded by setting the Failsafe error flag on the display.

h. Wait 400 milliseconds. This is long enough for the Failsafe Timer to have expired.

i. The data and ID are read to make sure they ARE the Failsafe values. Any results that are NOT the Failsafe values are recorded by setting the Failsafe error flag on the display.

```
                  Prom Programmer Performance Verification
                                  Failsafe
  Prom Programmer in card slot #   1

   Test          results    (cumulative results)              # Fail   # Test

 Failsafe timeout passed   (passed)                               0        0


 STATUS: Awaiting test selection __________________________________ 14:18

 -

  ________ ________ ________ _start__ exit_test ________ ________ _print__
```

Figure 4-6. Failsafe Test Display

4-25. The Failsafe Test exercises the following components on the Prom Control board:

Outward Transfer Path:

Address Block:

U3A, U3B, U8A	Latch
U2A, U2B	Diode Packs
RP1, RP2	Resistor Packs
UR1A, UR1B	Resistor Packs

Data Out Block:

U6B	Latch
U4A - U4D	Buffers
U5A - U5D	Buffers

Inward Transfer Path:

ID Block:

U3C	Buffer
U2C	Diode Pack (partials)
RP3	Resistor Pack
UR1C	Resistor Pack

Data In Block:

U6C	Buffer
U2C, U2D	Diode Pack (partials)
U3D, U3E	Comparators
RP4	Resistor Pack
UR1D	Resistor Pack

Non-transfer Path:

Failsafe Block:

U7D	NAND (partial)
U8D	Monostable Multivibrator
U8C	Counter
U7E	NOR (partial)

Cold Socket Block:

U8B	Flip-Flop (partial)
U7G	Buffer
U8F	Buffer

4-26. The Failsafe Test displays Pass/Fail information on the Failsafe Timer. If the Failsafe Timer fails, then it is assigned a fail tag; a pass tag means it has passed the test. If it fails, check the Failsafe Block and the Cold Socket Block.

4-27. SUPPLY ADJUST TEST. The "Supply Adjust" test only displays Pass/Fail information for the "VP3 overload test". All the other tests under "Supply Adjust" provide specific waveforms and voltage levels for measuring and adjusting the supplies. The "Supply Adjust" test requires an oscilloscope and voltmeter. The results cannot be determined to pass or fail unless the operator views the waveshapes on an oscilloscope and measures the voltage levels with a voltmeter.

```
                    Prom Programmer Performance Verification
                                 Supply Adjust
  Prom Programmer in card slot #   1

   Test                                                          # Test

 All supplies are powered for measurement and adjustment.           0

 VP3 Overload test (performed in above test)                0       0

 10 volt VP3                                                        0



 STATUS: Awaiting test selection ____________________________ 14:18

 -

 ______ __cycle__ next test __start__ exit test ______ ______ __print__
```

Figure 4-7. Supply Adjust Test

4-28. There are two tests; the "All supplies powered for measurement and adjustment" test, and the "10 volt VP3" test. Included in the first test is the "VP3 overload" test. (See figure 4-7). The following sequence is for operating the "10 volt VP3" test:

a. From the Keyboard call up the PROM Performance Verification. This is done by pressing the [opt_test] softkey followed by the RETURN key. A table will be displayed indicating the location of the option boards in the card cage of the mainframe. Press the number corresponding to the slot number which the PROM Controller board occupies followed by the RETURN key.

b. Press the [next_test] softkey until the "Supply Adjust" test is highlighted.

c. Press the [disp_test] softkey followed by the [next_test] softkey. Then press the [start] softkey to initializes the "10 volt VP3" test.

d. Measure the voltage at TP6. Adjust R34 for a voltage at TP6 between 4.65 and 5.3 volts. Now measure TP3 (VP3) for 10 volts +-.03 volts.

4-29. The second test "All supplies powered for measurement and adjustment" should now be performed. It is assumed that the "10 volt VP3" test was previously performed and the display is still under the "Supply Adjust" menu. The following is the operating procedure for the "All supplies powered for measurement and adjustment" test:

a. Press the [next_test] softkey until the "All supplies are powered for measurement and adjustment" test is highlighted.

d. Set up oscilloscope as follows:

CH A: DC....5v/Div. probe to TP3 on 64501A bd.
CH B: DC....5v/Div. probe to TP12

DISPLAY A
TRIGGER B

TRIGGER MODE: NORMAL
TRIGGER: POSITIVE SLOPE

TIME/DIV .5ms main

*** NOTE ***

All buttons on scope should be in the out position to start. All delay controls must be OFF and all calibrating controls in the detent position.

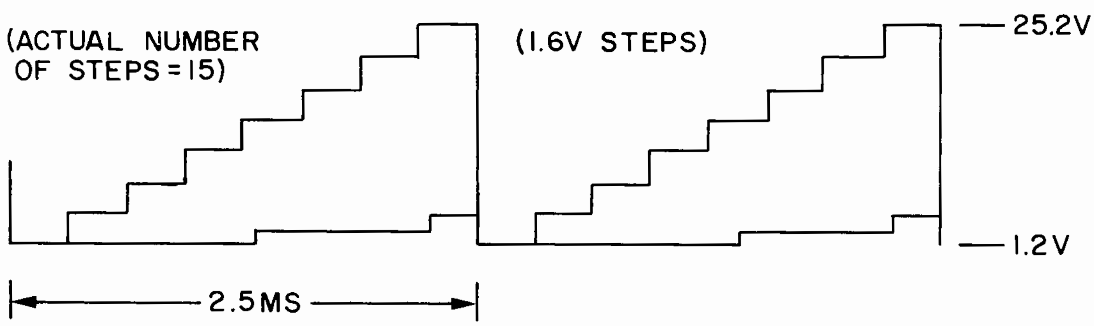


Figure 4-8. VP3 Waveform (1.2v - 26.7v)

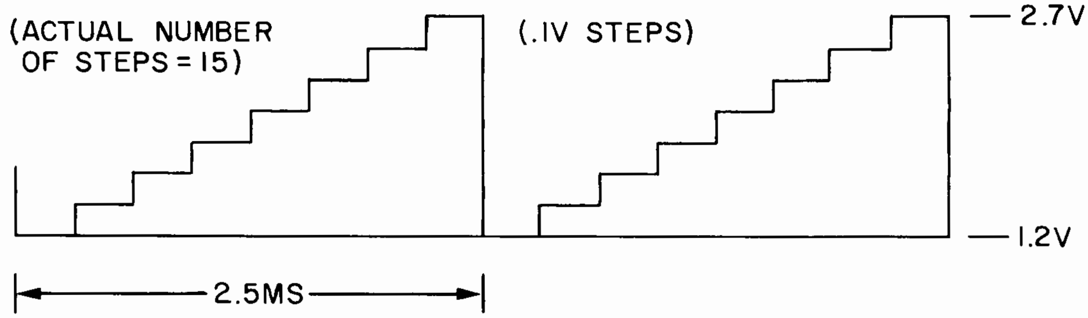


Figure 4-9. VP3 Waveform (1.2v - 2.8v)

e. VP3 is shaped into two ramps. The low end ramp steps from 1.2 to 2.7 volts in equal 0.1 volt increments. This is repeated 10 times. The high end ramp steps from 1.2 to 25.2 volts in equal 1.6 volt increments.

f. Adjust the trigger level for a stable trace. The top part of the waveform should look like figure 4-8. NOTE: The waveform MUST contain 15 steps and be linear.

g. Adjust Channel A for 1v/DIV. The bottom part of the waveform should look like figure 4-9. NOTE: The waveform MUST also contain 15 steps and be linear.

4-30. The "VP3 overload" test can be tested while running the "All supplies powered for measurement and adjustment". The "VP3 overload" test can not be directly accessed like the other two tests.

4-31. This test displays both the "# Test" and number of failures. The number of failures (the overload counter) is shown to the left of the "# Test" counter. (See figure 4-7).

4-32. The current overload bit is tested at the last rise of the high end ramp. If the overload bit is detected, the overload counter on the display will be incremented to reflect the overload. The procedure for checking this test is as follows:

a. Place one end of a 50 Ohm 1W resistor into the Prom ZIF socket hole 12 on the 64502A Module. Secure by pushing the ZIF socket insertion lever forward. With either the "All supplies powered for measurement and adjustment" test running, momentarily touch the other resistor lead to the PROM socket hole 21.

CAUTION

The 50 Ohm 1W resistor will get hot! The DAC is capable of approximately 15 watts.

b. The "VP3 overload test" should start counting overloads. This verifies that the overload detector U6F is operating.

4-33. TROUBLESHOOTING.

4-34. This section is to be used when one of the performance verification tests fails. Troubleshooting a failure on the 64501A board or any part of the mainframe should only be performed by qualified service personnel.

4-35. 64000 SYSTEM CRASH. If the 64000 crashes when the 64501A PROM Programmer Control board is placed in the card cage, then either a bad signal or short is present on the 64501A board.

4-36. To locate the problem, first, check the power supply input lines to the 64501A board for shorts. If this is not the problem, then place a ET19783 Extender board into the mainframe with the 64501A board installed in it. Open the address lines by opening switches S1 and S2 on the extender board. Press S7 (the LPOP switch) to see if the keyboard will respond to a key depressed. If the keyboard does respond to a keyboard input, then the problem lies with the address lines. Close the address lines one at a time until the keyboard does not respond anymore. The last address line closed is the problem. Open that line again and continue to close the other address lines to make sure that there are no other failures.

4-37. If the address lines are opened and the system does not recover when S7 on the extender board is pressed, then open the data lines by opening all the switches on S3 and S4. Press S7 to see if the system has now recovered. If the system does recover, then the failure lies with the data lines. Close the data lines one at a time until the keyboard responds to a key being depressed. The problem lies with the last data line that was closed when the keyboard was recognized.

4-38. If both the address and data lines are opened and the system still does not respond, then open the control lines (S5 and S6). Press S7. The system should now respond to the keyboard. If the system does respond to the keyboard, then close one control line at a time until it does not. The failure lies with the last control line closed.

4-39. If all the switches (S1 thru S6 on the extender board) are opened, and the system still does not respond, check the supply voltages. Remove the board and check again.

4-40. PERFORMANCE VERIFICATION FAILURE. Use the results of performance verification to determine which loop to start. Always start troubleshooting the first test to fail. If there is an error code message in the test, refer to the description of the test referred to previously in this section.

4-41. SIGNATURE ANALYSIS. Verify that the proper "Vh" signature is present by probing +5 volts in each signature analysis loop before starting.

4-42. Socket ID Test Signature Analysis. The Socket ID Test is entered when the 64502A Module's ID is not recognized. The socket ID Test can manually be entered by grounding U6A pin 12 before and while entering performance verification to access Signature Analysis Loop D. Take signatures on UR1A, UR1B, U4E, and U5E. If these are bad, then the failure is in the outward transfer path. If the signatures are good at UR1A and UR1B, then check the signatures at UR1C (inward transfer path). If these signatures are bad, then verify VP1, VP2, VP3 are at 1.2 volts, and check the connections to the 64502A Module. If the signatures are good at UR1C, then check U3C. If the signatures are bad at U3C, the problem is in U3C, the control circuit, or the bus. If the signatures are good at U3C, check U6A.

4-43. Address-ID Test Signature Analysis. The Address-ID Test is one of four tests that can be run if the 64502A Module's ID is recognized. This test is similar to the Socket ID Test. If a failure occurs during the Address-ID Test, use Signature Analysis "Loop A" to troubleshoot the failure. Take signatures at UR1A, UR1B, U4E, and U5E. these signatures are bad, the problem is in the outward transfer path. If these signatures are good at UR1A and UR1B, then check signatures at UR1C (inward transfer path). If they are bad, then check VP1, VP2, VP3, and the connections to the 64502A Module. If the signatures are good at UR1C, then check U3C. If the signatures are bad at U3C, then the problem is in U3C, the control circuit, or on the bus. If the signatures are good at U3C, check U6A.

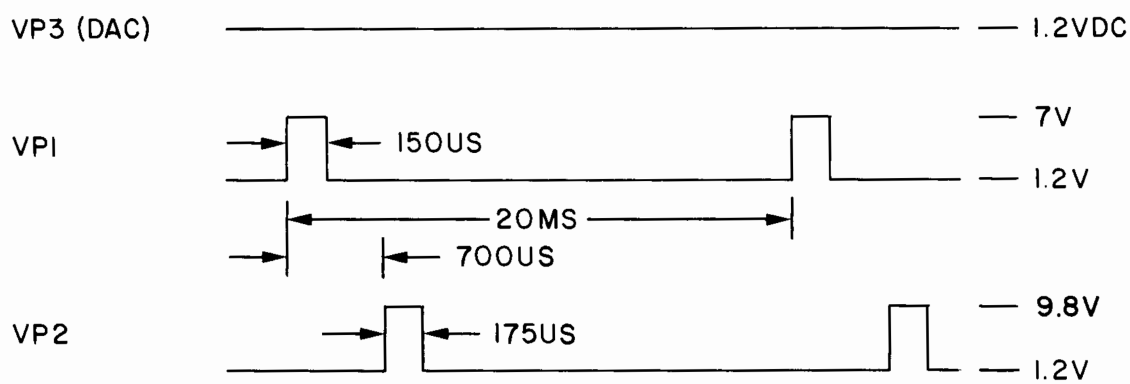


Figure 4-10. VP1, VP2, VP3 waveforms for the Address-ID Test

4-44. Data Test Signature Analysis. The Data Test is one of four performance verification tests that can be run if the 64502A Module's ID is recognized. If a failure occurs while running this test, troubleshoot the failure with Signature Analysis Loop B. Take signatures at U4A thru U4D, and U5A thru U5D. If these are bad, then the problem is in the outward transfer path. Check U6B. If the signatures are good, then check UR1D. If the signatures are bad at UR1D, then check the cable connections. If they are good at UR1D, then check U3E. If the signatures are bad at U3E, then the problem may be U3E. If the signatures are good at U3E, then check U6C. If these signatures are bad at U6C, then the problem may be U6C, the control circuit, or on the bus.

4-45. Supplies Test Signature Analysis. The Supplies Test is one of four performance verification tests that can be entered if the 64502A Module's ID is recognized. If a failure occurs while running this test, troubleshoot with Signature Analysis Loop C. Start taking signatures at UR1A, UR1B, U4E, U5E, and U7A. If these signatures are bad, then the problem is in the outward transfer path. If the signatures are good at UR1A and UR1B, check UR1C (inward transfer path). If these signatures are bad, check VP1, VP2, VP3, and the connections to the 64502A Module. If the signatures are good at UR1C, check U3C. If the signatures are bad at U3C, the problem may be U3C, the control circuitry, or the bus. If the signatures are good at U3C, check U6A.

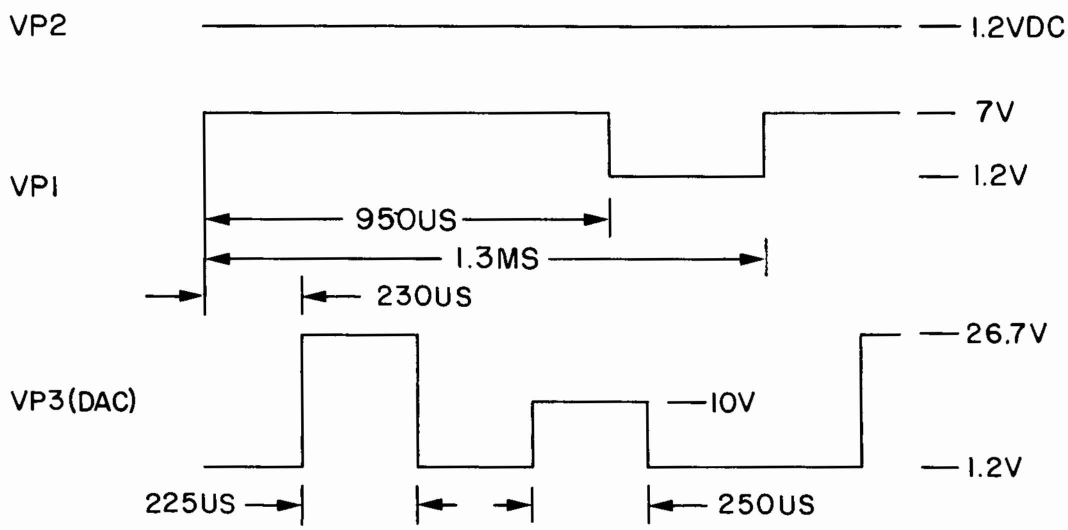


Figure 4-11. Waveforms for the Supplies Test

4-46. Failsafe Test Signature Analysis. The Failsafe Test does not have a signature analysis loop. It is used to verify that the Failsafe Timer is operating. To troubleshoot a failure that occurred in this test, use the "Supplies TEST" performance verification and Signature Analysis Loop C.

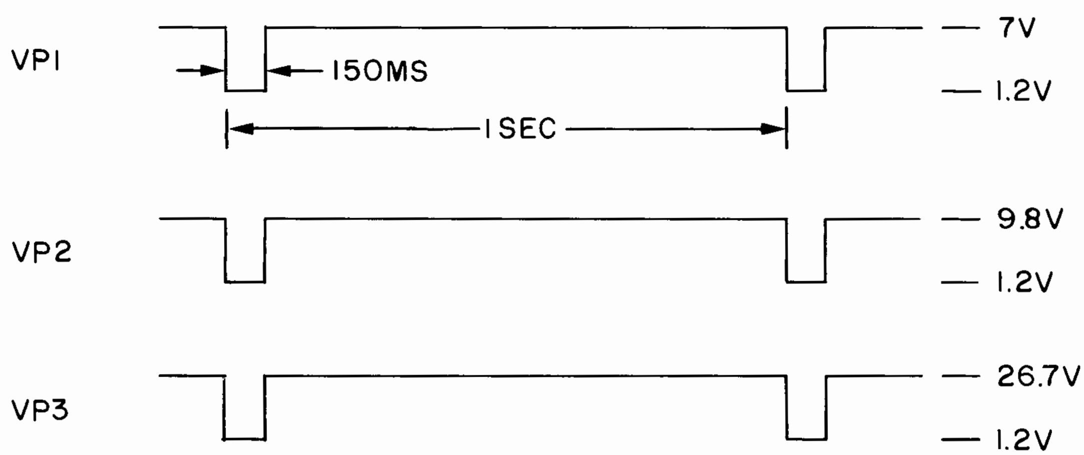


Figure 4-12. VP1, VP2, VP3 Waveforms for the Failsafe Test

4-47. Supply Adjust Test Signature Analysis. There is no signature analysis loop to troubleshoot the Supply Adjust Test. This test requires an oscilloscope and voltmeter for measurement and troubleshooting. If the VP3 (DAC) waveform is incorrect (see figure 13, 14), enter and [start] the "Supplies Test". Use signature analysis loop C. If there is an overload problem, then check the operation of U6F. If one of the other waveforms is incorrect, then check the signal path with a scope.

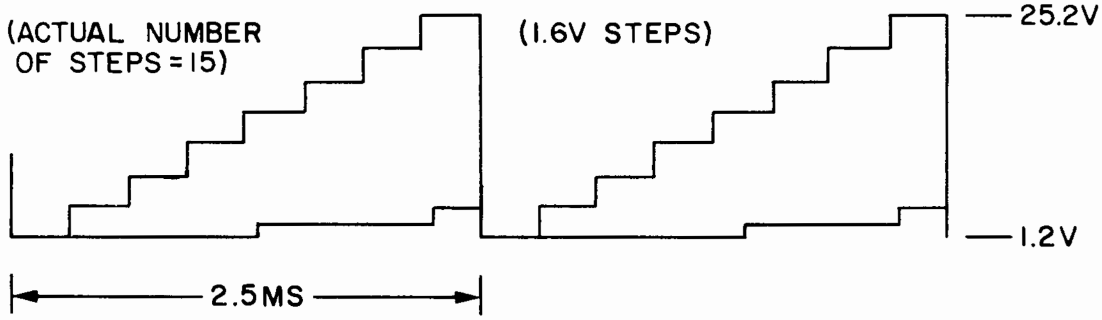


Figure 4-13. VP3 Waveform (1.2v - 26.7v)

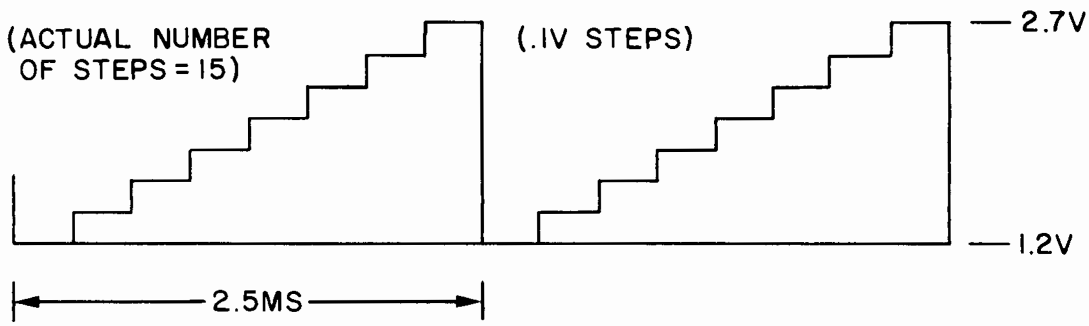


Figure 4-14. VP3 Waveform (1.2v - 2.8v)

Table 4-4. Signature Analysis Loop A

LOOP A - ADDRESS/ID

MODE = normal
CLOCK = neg. edge : TP9
START = neg. edge : TP12
STOP = pos. edge : TP12

Vh = 2A2C

NODE	SIG.
UR1A-1	C532
UR1A-2	346A
UR1A-3	3108
UR1A-4	228U
UR1A-5	1564
UR1A-6	F5U5
UR1A-7	U774
UR1A-8	3H71
UR1A-9	3H71
UR1A-10	U774
UR1A-11	F5U5
UR1A-12	1564
UR1A-13	228U
UR1A-14	3108
UR1A-15	346A
UR1A-16	C532
UR1B-1	0001
UR1B-2	060U
UR1B-3	C240
UR1B-4	5168
UR1B-5	FA8F
UR1B-6	FA92
UR1B-7	FAPA
UR1B-8	FC09
UR1C-4	68PC
UR1C-5	7383
UR1C-6	99PH
UR1C-7	56U2
UR1C-8	060U
UR1D-1	0000
UR1D-2	0000
UR1D-3	0000

NODE	SIG.
UR1D-4	0000
UR1D-5	0000
UR1D-6	0000
UR1D-7	0000
UR1D-8	0000
U3A-1	2A2C
TOTLZ=1	
U3A-3	F2HP
U3A-4	2743
U3A-7	A1H1
U3A-8	PPCC
U3A-11	FF32
U3A-13	7F3F
U3A-14	7232
U3A-17	280P
U3A-18	3P81
U3B-3	9710
U3B-4	2AAA
U3B-7	2A0C
U3B-8	2A23
U3B-12	5168
U3B-13	0U53
U3B-14	8C33
U3B-15	C240
U3B-17	F426
U3B-18	FF30
U3C-1	5927
U3C-11	2A2C
TOTLZ=2	
U3D-1	0000
U3D-2	0000

NODE	SIG.
U3D-13	0000
U3D-14	0000
U3E-1	0000
U3E-2	0000
U3E-13	0000
U3E-14	0000
U4A-1	0000
U4A-3	0000
U4B-1	0000
U4B-3	0000
U4C-1	0000
U4C-3	0000
U4D-1	0000
U4D-3	0000
U4E-3	060U
U5A-1	0000
U5A-3	0000
U5B-1	0000
U5B-3	0000
U5C-1	0000
U5C-3	0000
U5D-1	0000
U5D-3	0000
U5E-3	0001

Table 4-4. Signature Analysis Loop A (Cont'd)

NODE	SIG.
U6A-1	5927
U6A-2	F2HP
U6A-3	3P81
U6A-4	2743
U6A-5	280P
U6A-6	A1H1
U6A-7	7232
U6A-8	PPCC
U6A-9	7F3F
U6A-19	0000
TOTLZ=1	
U6B-11	2A2C
TOTLZ=1	
U6C-1	2A2C
U6D-2	2A2C
U6D-4	P619
U6D-6	730F
U6D-8	730F
U6D-9	0000
U6D-11	0000
U6D-12	730F
U6D-14	730F
U6D-16	P619
U6D-18	0000
U6E-2	2A2C
U6E-3	0000
U6E-4	2A2C
U6E-6	2A2C
U6E-7	0000
U6E-13	0U53
U7B-2	9710
U7B-4	2AAA
U7B-6	2A0C
U7B-8	2A23
U7B-13	8C33
U7B-15	F426
U7B-17	FF30
U7C-6	2A2C
TOTLZ=43	
U7C-10	2A2C
U7C-11	2A2C
TOTLZ=1	
U7C-13	2A2C
TOTLZ=1	
U7C-15	9515
U7D-8	CU3P
U7E-5	0000
U7F-3	060U
U7F-5	0001
U7G-3	0000
TOTLZ=1	
U7G-6	0000
TOTLZ=1	
U7G-8	2A2C
TOTLZ=1	
U7G-9	0000
TOTLZ=1	
U7G-11	2A2C
TOTLZ=1	
U8A-2	0000
U8A-5	0000
U8A-6	0000
U8A-9	0000
U8A-12	0000
U8A-15	0000
U8A-16	0000
U8A-19	0000
U8B-4	2A2C
U8C-6	0000
U8D-2	2A2C
U8F-2	2A2C
TOTLZ=1	
U8F-4	2A2C
TOTLZ=1	
TP12	0000
TOTLZ=1	

Table 4-5. Signature Analysis Loop B

LOOP B - DATA

MODE = normal
CLOCK = neg. edge : TP9
START = neg. edge : TP12
STOP = pos. edge : TP12

Vh = 5U91

NODE	SIG.
UR1A-1	0000
UR1A-2	0000
UR1A-3	0000
UR1A-4	0000
UR1A-5	0000
UR1A-6	0000
UR1A-7	0000
UR1A-8	0000
UR1A-9	0000
UR1A-10	0000
UR1A-11	0000
UR1A-12	0000
UR1A-13	0000
UR1A-14	0000
UR1A-15	0000
UR1A-16	0000
UR1B-1	0000
UR1B-2	0000
UR1B-3	0000
UR1B-4	0000
UR1B-5	0000
UR1B-6	0000
UR1B-7	0000
UR1B-8	0000
UR1C-4	5U91
UTOTLZ=1	
UR1C-5	5U91
UTOTLZ=1	
UR1C-6	5U91
UTOTLZ=1	
UR1C-7	5U91
UTOTLZ=1	
UR1C-8	0000

NODE	SIG.
UR1D-1	6U44
UR1D-2	19CU
UR1D-3	01PP
UR1D-4	H1H1
UR1D-5	C502
UR1D-6	C799
UR1D-7	AH47
UR1D-8	98PU
U3A-1	5U91
U3A-3	C9AA
U3A-4	H2UC
U3A-7	P747
U3A-8	P271
U3A-11	5U91
TOTLZ=1	
U3A-13	2CH6
U3A-14	8CA9
U3A-17	CC0C
U3A-18	56UF
U3B-3	AUF8
U3B-4	5U91
U3B-7	5U91
U3B-8	5U91
U3B-12	0000
U3B-13	5U91
U3B-14	5U91
U3B-15	0000
U3B-17	5U91
U3B-18	5U91
U3C-1	5U91
U3C-11	5U91

NODE	SIG.
U3D-1	AH47
U3D-2	98PU
U3D-13	C502
U3D-14	C799
U3E-1	01PP
U3E-2	H1H1
U3E-13	6U44
U3E-14	19CU
U4A-1	98PU
U4A-3	98PU
U4B-1	C502
U4B-3	C502
U4C-1	H1H1
U4C-3	H1H1
U4D-1	19CU
U4D-3	19CU
U4E-3	0000
U5A-1	AH47
U5A-3	AH47
U5B-1	C799
U5B-3	C799
U5C-1	01PP
U5C-3	01PP
U5D-1	6U44
U5D-3	6U44
TOTLZ=1	

Table 4-5. Signature Analysis Loop B (Cont'd)

NODE	SIG.
U5E-3	0000
U6A-1	0C09
U6A-2	C9AA
U6A-3	56UF
U6A-4	H2UC
U6A-5	CC0C
U6A-6	P747
U6A-7	8CA9
U6A-8	P271
U6A-9	2CH6
U6A-19	0000
U6B-11	U6A1
U6C-1	0C09
U6D-2	5U91
U6D-4	UHA8
U6D-6	UHA8
U6D-8	5498
U6D-9	0000
U6D-11	0000
U6D-12	5498
U6D-14	UHA8
U6D-16	UHA8
U6D-18	0000
U6E-2	5U91
U6E-3	0000
U6E-4	5U91
U6E-6	5U91
U6E-7	0000
U6E-13	5U91

NODE	SIG.
U7B-2	AUF8
U7B-4	5U91
U7B-6	5U91
U7B-8	5U91
U7B-13	5U91
U7B-15	5U91
U7B-17	5U91
U7C-6	5U91
TOTLZ=776	
U7C-10	5U91
TOTLZ=1	
U7C-11	5U91
TOTLZ=1	
U7C-13	5U91
TOTLZ=1	
U7C-15	UHA8
U7D-8	A239
U7E-5	0000
U7F-3	0000
U7F-5	0000
U7G-3	0000
TOTLZ=1	
U7G-6	0000
TOTLZ=1	
U7G-8	5U91
TOTLZ=1	
U7G-9	0000
TOTLZ=1	
U7G-11	5U91

NODE	SIG.
U8A-2	0000
U8A-5	0000
U8A-6	0000
U8A-9	0000
U8A-12	0000
U8A-15	0000
U8A-16	0000
U8A-19	0000
U8B-4	5U91
U8C-6	0000
U8D-2	5U91
U8F-2	5U91
TOTLZ=1	
U8F-4	5U91
TOTLZ=1	
TP12	0000
TOTLZ=1	

Table 4-6. Signature Analysis Loop C

LOOP C - SUPPLIES

MODE = normal
CLOCK = neg. edge : TP9
START = neg. edge : TP12
STOP = pos. edge : TP12

Vh = C4C6

NODE	SIG.
UR1A-1	6H2H
UR1A-2	6H2H
UR1A-3	6H2H
UR1A-4	6H2H
UR1A-5	6H2H
UR1A-6	6H2H
UR1A-7	6H2H
UR1A-8	6H2H
UR1A-9	6H2H
UR1A-10	6H2H
UR1A-11	6H2H
UR1A-12	6H2H
UR1A-13	6H2H
UR1A-14	6H2H
UR1A-15	6H2H
UR1A-16	6H2H
UR1B-1	0000
UR1B-2	0FC7
UR1B-3	6H2H
UR1B-4	6H2H
UR1B-5	6H2H
UR1B-6	6H2H
UR1B-7	6H2H
UR1B-8	6H2H
UR1C-4	H99C
UR1C-5	H99C
UR1C-6	C46F
UR1C-7	C8HC
UR1C-8	0FC7
UR1D-1	0000
UR1D-2	0000
UR1D-3	0000

NODE	SIG.
UR1D-4	0000
UR1D-5	0000
UR1D-6	0000
UR1D-7	0000
UR1D-8	0000
U3A-1	C4C6
U3A-3	UH95
U3A-4	UFA5
U3A-7	460H
U3A-8	6AA7
U3A-11	1F4F
U3A-13	7847
U3A-14	HAPC
U3A-17	HUF1
U3A-18	HPAC
U3B-3	C12F
U3B-4	HUF1
U3B-7	HUF1
U3B-8	HUF1
U3B-12	6H2H
U3B-13	HUF1
U3B-14	HUF1
U3B-15	6H2H
U3B-17	68C7
U3B-18	773C
U3C-1	1330
U3C-11	C4C6
TOTLZ=2	
U3D-1	0000
U3D-2	0000
U3D-13	0000

NODE	SIG.
U3D-14	0000
U3E-1	0000
U3E-2	0000
U3E-13	0000
U3E-14	0000
U4A-1	0000
U4A-3	0000
U4B-1	0000
U4B-3	0000
U4C-1	0000
U4C-3	0000
U4D-1	0000
U4D-3	0000
U4E-3	0FC7
U5A-1	0000
U5A-3	0000
U5B-1	0000
U5B-3	0000
U5C-1	0000
U5C-3	0000
U5D-1	0000
U5D-3	0000
U5E-3	0000

Table 4-6. Signature Analysis Loop C (Cont'd)

NODE	SIG.
U6A-1	1330
U6A-2	UH95
U6A-3	HAPC
U6A-4	UFA5
U6A-5	HUF1
U6A-6	460H
U6A-7	HAPC
U6A-8	6AA7
U6A-9	7847
U6A-19	0000
U6B-11	C4C6
TOTLZ=1	
U6C-1	C4C6
U6D-2	0000
U6D-4	A8UA
U6D-6	UH53
U6D-8	A786
U6D-9	0000
U6D-11	0000
U6D-12	A786
U6D-14	UH53
U6D-16	A8UA
U6D-18	0000
U6E-2	C4C6
U6E-3	0000
U6E-4	C4C6
U6E-6	C4C6
U6E-7	0000
U6E-13	HUF1
U7B-2	C12F

NODE	SIG.
U7B-4	HUF1
U7B-6	HUF1
U7B-8	HUF1
U7B-13	HUF1
U7B-15	68C7
U7B-17	773C
U7C-6	C4C6
TOTLZ=100	
U7C-10	C4C6
TOTLZ=2	
U7C-11	C4C6
TOTLZ=1	
U7C-13	PP63
U7C-15	55A9
U7D-8	P11U
U7E-5	0000
U7F-3	0FC7
U7F-5	0000
U7G-3	0000
TOTLZ=1	
U7G-6	0000
TOTLZ=1	
U7G-8	C4C6
TOTLZ=1	
U7G-9	0000
TOTLZ=1	
U7G-11	C4C6
TOTLZ=1	
U8A-2	UF3F

NODE	SIG.
U8A-5	UF3F
U8A-6	UF3F
U8A-9	00HA
U8A-12	00HA
U8A-15	UF3F
U8A-16	00HA
U8A-19	UF3F
U8B-4	C4C6
U8C-6	0000
U8D-2	C4C6
U8F-2	C4C6
TOTLZ=1	
U8F-4	C4C6
TOTLZ=1	
TP12	0000
TOTLZ=1	

Table 4-7. Signature Analysis Loop D

LOOP D - SOCKET ID

MODE = normal
CLOCK = neg. edge : TP9
START = neg. edge : TP12
STOP = pos. edge : TP12

NOTE: Ground U6A pin 12 before and while entering performance verification to manually access Signature Analysis Loop D.

Vh = P672

NODE	SIG.	NODE	SIG.	NODE	SIG.
UR1A-1	596C	UR1D-3	0000	U3D-13	0000
UR1A-2	CA43	UR1D-4	0000	U3D-14	0000
UR1A-3	36P3	UR1D-5	0000		
UR1A-4	0462	UR1D-6	0000	U3E-1	0000
UR1A-5	21A1	UR1D-7	0000	U3E-2	0000
UR1A-6	39UF	UR1D-8	0000	U3E-13	0000
UR1A-7	381U			U3E-14	0000
UR1A-8	3U93	U3A-1	P672		
UR1A-9	3U93	TOTLZ=1		U4A-1	0000
UR1A-10	381U	U3A-3	65FF	U4A-3	0000
UR1A-11	39UF	U3A-4	CF62		
UR1A-12	21A1	U3A-7	A02A	U4B-1	0000
UR1A-13	0462	U3A-8	H71P	U4B-3	0000
UR1A-14	36P3	U3A-11	445F		
UR1A-15	CA43	U3A-13	6367	U4C-1	0000
UR1A-16	596C	U3A-14	PP77	U4C-3	0000
		U3A-17	P472		
UR1B-1	0000	U3A-18	P6U3	U4D-1	0000
UR1B-2	0000			U4D-3	0000
UR1B-3	399C	U3B-3	7339		
UR1B-4	3985	U3B-4	P672	U4E-3	0000
UR1B-5	399F	U3B-7	P672		
UR1B-6	399F	U3B-8	P672	U5A-1	0000
UR1B-7	399F	U3B-12	3985	U5A-3	0000
UR1B-8	399F	U3B-13	P650		
		U3B-14	P678	U5B-1	0000
UR1C-4	1196	U3B-15	399C	U5B-3	0000
UR1C-5	0P47	U3B-17	445F		
UR1C-6	04C9	U3B-18	445F	U5C-1	0000
UR1C-7	8U95			U5C-3	0000
UR1C-8	0000	U3C-1	3765		
TOTLZ=1		U3C-11	P672	U5D-1	0000
				U5D-3	0000
UR1D-1	0000	U3D-1	0000		
UR1D-2	0000	U3D-2	0000	U5E-3	0000

Table 4-7. Signature Analysis Loop D (Cont'd)

NODE	SIG.
U6A-1	3765
U6A-2	65FF
U6A-3	P6U3
U6A-4	CF62
U6A-5	P472
U6A-6	A02A
U6A-7	PP77
U6A-8	H71P
U6A-9	6367
U6A-19	0000
U6B-11	P672
TOTLZ=1	
U6C-1	P672
U6D-2	P672
U6D-4	A22P
U6D-6	H117
U6D-8	H117
U6D-9	0000
U6D-11	0000
U6D-12	H117
U6D-14	H117
U6D-16	A22P
U6D-18	P672
U6E-2	P672
U6E-3	0000
U6E-4	P672
U6E-6	P672
U6E-7	0000
U6E-13	P650
U7B-2	7339

NODE	SIG.
U7B-4	P672
U7B-6	P672
U7B-8	P672
U7B-13	P678
U7B-15	445F
U7B-17	445F
U7C-6	P672
TOTLZ=31	
U7C-10	P672
TOTLZ=1	
U7C-11	P672
TOTLZ=1	
U7C-13	P672
TOTLZ=1	
U7C-15	7339
U7D-8	954C
U7E-5	0000
U7F-3	0000
U7F-5	0000
U7G-3	0000
TOTLZ=1	
U7G-6	0000
TOTLZ=1	
U7G-8	P672
TOTLZ=1	
U7G-9	0000
TOTLZ=1	
U7G-11	P672
TOTLZ=1	

NODE	SIG.
U8A-2	0000
U8A-5	0000
U8A-6	0000
U8A-9	0000
U8A-12	0000
U8A-15	0000
U8A-16	0000
U8A-19	0000
U8B-4	P672
U8C-6	0000
U8D-2	P672
U8F-2	P672
TOTLZ=1	
U8F-4	P672
TOTLZ=1	
TP12	0000
TOTLZ=1	

SECTION V

ADJUSTMENT PROCEDURE

5-1. INTRODUCTION.

5-2. This section describes the adjustment required to return the +5 volt supply to operating specification after repairs have been made. The other supplies (+12, -12, -5, and 40 volt) have no adjustment.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with International Safety Standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summery at the front of this manual or with specific warnings given throughout the manual could result in serious injury or death. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

5-6. A Voltmeter capable of .01 Volts DC accuracy is required for the adjustment procedure.

5-7. ADJUSTMENTS.

5-8. The +5 volt supply is the only supply that can be adjusted. The +5 volts is derived from the +12 volt supply by voltage regulator VR1.

5-9. The following are the steps that must be taken before measurement and adjustment of the +5 volt supply can be started:

a) Get into Prom Performance Verification. To do this press the [opt_test] softkey. Then type in the slot number which the Prom Programmer Control board occupies (the display will show which slot it is in), followed by the RETURN key.

b) Press the [next_test] softkey until the "Supply Adjust" Test is highlighted.

c) Press the [disp_test] softkey. The "All supplies are powered for measurement and adjustment" will be highlighted. Press the [next_test] softkey until the "10 Volt VP3" test is highlighted.

d) Press the [start] softkey to initiate the test. This test stimulates VP3 at TP3 (DAC) and the +5 volt supply for measurement and adjustment.

5-10. Place the Voltmeter on TP3 and measure VP3. Adjust the voltage with R34 to between 9.97 and 10.03 volts.

5-11. Place the Voltmeter on TP6 and measure the voltage. It should be between 4.65 and 5.3 volts.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one, all in capital letters; and two, partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous parts.

6-7. The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer of the part.

e. The manufacturer's part number.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-8. ORDERING INFORMATION.

6-9. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/ Service Office.

6-10. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-11. DIRECT MAIL ORDER SYSTEM.

6-12. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No Maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP Office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-13. Mail-order forms and specific ordering information are available through your local HP Sales/Service Office. Addresses and phone numbers are located at the back of this manual.

SECTION VII

MANUAL BACKDATING

7-1. This section contains information for adapting this manual to the 64501A with Repair Numbers Prefixed 2239A that have a 64501-66502 board and software with a revcode of 2406A or later. If the software is not revcoded 2406A or later, then use the 64500-90910 service manual.

Section IV and Section VIII,
Replace: Replace/use to Backdate Manual for the 64501-66502 board.

SECTION IV

PERFORMANCE VERIFICATION AND TROUBLESHOOTING

4-1. INTRODUCTION.

4-2. The performance verification tests verify to approximately an 85% confidence level that the 64501A board are operational. With the addition of the Supply Adjust Test (which consists of the DAC output, the +10 volt VP3, and the VP3 Overload Detection Tests), the confidence level can be raised to approximately 98%. The Supply Adjust Test should only be performed by qualified Service Personnel.

4-3. There are five performance verification tests that verify if the PROM Programmer Control board and 64502A Module are operating properly. These tests are: The Address-ID test, the Data test, the Supplies test, the Failsafe test, and the Supply Adjust test. Each test will be explained in this section.

4-4. The Address-ID, Data, and the Supplies test all have signature analysis associated with them. If the ID for the Prom Programmer is not read correctly, then the ID test will automatically be entered. It too has a signature analysis loop for troubleshooting (see table 4-1).

Table 4-1. Available Signature Analysis Loops

Loop A	-	Run the "Address-ID" Performance Verification Test
Loop B	-	Run the "Data" Performance Verification Test
Loop C	-	Run the "Supplies" Performance Verification Test
Loop D	-	Can only be stimulated when an ID failure occurs

*** When taking signatures, make sure the [start] softkey is used to ***
*** initiate signature analysis stimulus and not the [cycle] softkey. ***

4-5. EQUIPMENT REQUIRED.

4-6. A Model 5005A/B Signature Analyzer, Oscilloscope and ET19783 Extender board are required to troubleshoot the 64501A board.

4-7. The HP Model 64502A Programmer Module must be installed when running the PROM Programmer Control board Performance Verification. See the 64502A Service Manual for the installation procedure.

NOTE

The Model 64502A PROM Module is the only module that can be used to run Performance Verification on the 64501A PROM Programmer Control board. Other PROM Programmer Modules have different ID's than the 64502A and will not enable the performance verification. Since the wrong ID would be called up, the system software will treat it as an ID failure and automatically enter into the ID Test.

4-8. If a problem does occur, refer to the Performance Verification theory for an understanding of its operation. This will help in troubleshooting the 64501A PROM Programmer Control board and the 64502A Prom Module.

4-9. RUNNING THE PERFORMANCE VERIFICATION.

a. From the Keyboard call up the PROM Performance Verification. This is done by pressing the [opt_test] softkey followed by the RETURN key. A table will be displayed indicating the location of the option boards in the card cage of the mainframe. Press the number corresponding to the slot number which the PROM Controller board occupies followed by the RETURN key.

b. Press the [cycle] softkey to run the Performance Verification on the first four tests. The fifth test (Supply Adjust) is a measurement and adjustment test. An oscilloscope/voltmeter is required for this test Note the Pass/Fail response. If a failure occurs then troubleshoot that failure with signature analysis.

4-10. PERFORMANCE VERIFICATION THEORY.

4-11. The Prom Programmer Control board circuitry is effectively tested by the performance verification software to approximately an 85% confidence level. If one of the performance verification tests does not pass, set up and use signature analysis to troubleshoot the failure. Only qualified Service Personnel should troubleshoot a failure.

```
                      Prom Programmer Performance Verification

    Prom Programmer in card slot #    1

     Test                                                        # Fail   # Test

    Address-ID                                                      0        0

    Data                                                            0        0

    Supplies                                                        0        0

    Failsafe                                                        0        0

    Supply Adjust                                                  N/A       0






   STATUS: Awaiting test selection ________________________________________ 14:18

   _

    ___end___ __cycle__ next test  dsp test ________ _________ _________ __print__
```

Figure 4-1. Prom Programmer Performance Verification Display

4-12. PRELIMINARY ID TEST. The ID Test is only entered when the 64502A Prom Prom Programmer Module's ID is not recognized or another module is used instead. Performance verification can ONLY be run on the 64501A Prom Programmer Control board when the 64502A module is attached. If the correct ID code (01H) is not read from the module, then the main selection of tests is not displayed. Instead, a limited ID test is offered where the address latches are set up to a specific pattern and a certain ID code is expected to be read according to the following pairs:

Table 4-2. ID Test Code

HEX ADDRESS	HEX DATA
C000	19
C001	01
C002	03
C004	05
C008	07
C010	09
C020	0B
C040	0D
C080	0F
D000	39
E000	59
F000	79

```
Prom Programmer Performance Verification

Prom Programmer in card slot #   1

Test                                                  # Fail   # Test

Socket ID                                                0        0

64502A prom module ID not detected-only ID test may be run






STATUS: Awaiting option_test command ________________________ 14:18


__end__ _______ _______ __dsp test__ _______ _______ _______ __print__
```

Figure 4-2. ID Test Display

4-13. The ID Test exercises the following components on the board:

Outward Transfer Path:

Address Block:

U5, U13	Latch
U2, U12	Diode packs
U3, U4	Resistor Packs
U1, U11	Resistor Packs

Inward Transfer Path:

ID Block:

U9	Latch
U7	Diode Pack
U8	Resistor Pack
U6	Resistor Pack

4-14. The ID Test displays Pass/Fail information on the 7 bits of data from the ID Buffer. If any bit fails, then its bit position is assigned a "1" value. A "0" value means it has passed the test. The least significant bit refers to the data path which ends at U9-18 and is sourced from VR4. The MSB refers to the data path of U9-12. There is a combination of address lines, VP1, VP2, and VP3 which influence the upper 6 bits. If failures occur on U22, U16, VR3, or or VR4 this test could fail (only on some bits).

4-15. ADDRESS-ID TEST. The Address-ID Test outputs to the address latches and then reads from the ID lines in the same way that the ID Tests does, but it adds more pairs of data. The following is a list of the data pairs:

Table 4-3. Address Latch Data Pairs

HEX ADDRESS	HEX DATA
C000	19
C001	01
C002	03
C004	05
C008	07
C010	09
C020	0B
C040	0D
C080	0F
D000	39
E000	59
F000	79
8001	00
C100	11
C200	13
C400	15
C800	17
4000	0F

4-16. The Address-ID Test exercises the following components on the board:

Outward Transfer Path:

Address Block:

U5, U13	Latch
U2, U12	Diode Packs
U3, U4	Resistor Packs
U1, U11	Resistor Packs

Others:

U22, U16	Buffer
VR2, VR4	Adjustable Voltage Regulators

Inward Transfer Path:

ID Block:

U9	Latch
U7	Diode Pack (partial)
U8	Resistor Pack
U6	Resistor Pack

4-17. The Address-ID Test gives Pass/Fail information on the 7 bits of data from the ID Buffer. If any bit fails, then its bit position is assigned a "1" value. A "0" value means it has passed the test. The least significant bit refers to the data path which ends at U9-18 and is sourced from VR4. The MSB refers to the data path of U9-12. There is a combination of address lines, VP1, VP2, and VP3 which influence the upper 6 bits.

```
                    Prom Programmer Performance Verification
                                   Address-ID
 Prom Programmer in card slot #   1

  Test          results    (cumulative results)                  # Fail   # Test

 ID buffer       0000000    (0000000)                                 0        0


 STATUS: Awaiting test selection ______________________________________ 14:18

 _______ _______ _______ __start__ exit test _______ _______ __print__
```

Figure 4-3. Address-ID Test Display

4-18. DATA TEST. The Data Test outputs the data sequence 0000 thru 00FFH to the Prom Programmer data register and reads back the data expecting to the same sequence.

```
                 Prom Programmer Performance Verification
                                Failsafe
  Prom Programmer in card slot #   1

   Test          results   (cumulative results)           # Fail  # Test

 Failsafe timeout passed   (passed)                           0       0






 STATUS: Awaiting test selection ______________________________ 14:18

 _

  ________ ________ ________ __start__ exit test ________ ________ __print__
```

Figure 4-4. Data Test Display

4-19. The Data Test exercises the following components on the board:

Outward Transfer Path:

Data Out Block:

U31	Latch
U30, U28, U26, U24	Buffers
U29, U27, U25, U23	Buffers

Inward Transfer Path:

Data In Block:

U20	Buffer
U7, U17	Diode Pack
U19, U18	Comparators
U15	Resistor Pack
R7-R14	Pull-up Resistors

4-20. The Data Test gives Pass/Fail information on the 8 bits of data from the Data Buffer. If any bit fails, then its bit position is assigned a "1" value. A "0" value means it has passed the test. The least significant bit refers to the data path which ends at U20-18 and is sourced from U31-3. The MSB refers to the data path of U20-9 and U31-18.

4-21. SUPPLIES TEST. The Supplies Test uses the ID lines to determine if the supplies are working.

NOTE

> The Prom Programmer Control board controls power to the Prom module.

The following tests are repeated 10 times to give a better scope presentation:

a. Address register set to 3FFFH, VP3 set to 1.2 volts. Reads the ID bits. Test the ID result to see that VP1 was low.

b. Address register set to 7FFFH, VP3 still at 1.2 volts. Reads the ID bits. Test the ID result to see that VP1 was high.

c. Address register remains at 7FFFH, VP3 is set to its maximum voltage of 26.7 volts. Reads the ID bits. Test the ID result to see tat VP3 was high, and that VP2 was low.

d. Address register remains at 7FFFH, VP3 is set to its minimum voltage of 1.2 volts. Reads the ID bits. Test the ID result to see that VP3 was low.

```
                     Prom Programmer Performance Verification
                                  Supplies
  Prom Programmer in card slot #   1

   Test          results    (cumulative results)                  # Fail   # Test

  VP1 test       passed     (passed)                                  0        0

  VP2 test       passed     (passed)

  VP3 test       passed     (passed)


  STATUS: Awaiting test selection ________________________________________ 14:18

  -

  _________ _________ _________ __start__ exit test _________ _________ __print__
```

Figure 4-5. Supplies Test Display

4-22. The Supplies Test exercises the following components on the board:

Outward Transfer Path:

Address Block:

U5, U13, U10	Latch
U2, U12	Diode Packs
U3, U4	Resistor Packs
U1, U11	Resistor Packs

DAC Block:

U10	Latch
U21	Digital to Analog Converter
U32	Op Amp
VR2	Adjustable Voltage Regulators

Others:

VR3, VR4	Adjustable Voltage Regulators
U22, U16	Buffer

Inward Transfer Path:

ID Block:

U20	Buffer
U7, U17	Diode Pack (partials)
U19, U18	Comparators
U15	Resistor Pack
R7-14	Pull-up Resistors

4-23. The Supplies Test displays Pass/Fail information on the three controllable supplies called VP1, VP2, and VP3. If any controllable supply fails, then it is assigned a fail tag on the display. A pass tag means it has passed the test. If VP3 fails, check the DAC block.

4-24. FAILSAFE TEST. The Failsafe Test checks the failsafe timer to make sure it responds in the proper time frame and that it can be reset with software control. The following test sequence is used:

a. The address lines are set to 0, data lines set to 0, and VP3 set at 26.7 volts (maximum voltage).

b. The data and ID are read to make sure they are not the Failsafe values. Any results that are the Failsafe values are recorded by setting the Failsafe error flag on the display.

c. Wait 400 milliseconds. This is too short for the Failsafe to have expired.

d. The data and ID are read to make sure they are not the Failsafe values. Any results that are the Failsafe values are recorded by setting the Failsafe error flag on the display.

e. The Failsafe Timer is reset so that it will not expire for at least another 500 milliseconds.

f. Wait 400 milliseconds more. This is too short for the Failsafe to have expired since it was reset.

g. The data and ID are read to make sure they are not the Failsafe values. Any results that are the Failsafe values are recorded by setting the Failsafe error flag on the display.

h. Wait 400 milliseconds. This is long enough for the Failsafe Timer to have expired.

i. The data and ID are read to make sure they ARE the Failsafe values. Any results that are NOT the Failsafe values are recorded by setting the Failsafe error flag on the display.

```
                    Prom Programmer Performance Verification
                                      Data
   Prom Programmer in card slot #   1

    Test           results    (cumulative results)                  # Fail  # Test

   Data buffer     00000000   (00000000)                               0       0

   STATUS: Awaiting test selection _______________________________________ 14:18

   -

   _________ _________ _________ __start__ exit test _________ _________ __print__
```

Figure 4-6. Failsafe Test Display

4-25. The Failsafe Test exercises the following components on the Prom Control board:

Outward Transfer Path:

Address Block:

U5, U13, U10	Latch
U2, U12	Diode Packs
U3, U4	Resistor Packs
U1, U11	Resistor Packs

Data Out Block:

U31	Latch
U30, U28, U26, U24	Buffers
U29, U27, U25, U23	Buffers

Inward Transfer Path:

ID Block:

U20	Buffer
U7, U17	Diode Pack (partials)
U19, U18	Comparators
U15	Resistor Pack
R7-14	Pull-up Resistors

Data In Block:

U20	Buffer
U7, U17	Diode Pack (partials)
U19, U18	Comparators
U15	Resistor Pack
R7-14	Pull-up Resistors

Non-transfer Path:

Failsafe Block:

U33	NAND (partial)
U40	Monostable Multivibrator
U40	Counter

4-26. The Failsafe Test displays Pass/Fail information on the Failsafe Timer. If the Failsafe Timer fails, then it is assigned a fail tag; a pass tag means it has passed the test.

4-27. SUPPLY ADJUST TEST. The "Supply Adjust" test only displays Pass/Fail information for the "VP3 overload test". All the other tests under "Supply Adjust" provide specific waveforms and voltage levels for measuring and adjusting the supplies. The "Supply Adjust" test requires an oscilloscope and voltmeter. The results cannot be determined to pass or fail unless the operator views the waveshapes on an oscilloscope and measures the voltage levels with a voltmeter.

```
              Prom Programmer Performance Verification
                           Supply Adjust
  Prom Programmer in card slot #   1

   Test                                                        # Test

  All supplies are powered for measurement and adjustment.          0

  VP3 Overload test (performed in above test)             0         0

  10 volt VP3                                                       0


  STATUS: Awaiting test selection ____________________________ 14:18

  -

  ________ __cycle__ next_test __start__ exit_test ________ ________ __print__
```

Figure 4-7. Supply Adjust Test

4-28. There are two tests; the "All supplies powered for measurement and adjustment" test, and the "10 volt VP3" test. Included in the first test is the "VP3 overload" test. (See figure 4-7). The following sequence is for operating the "10 volt VP3" test:

a. From the Keyboard call up the PROM Performance Verification. This is done by pressing the [opt_test] softkey followed by the RETURN key. A table will be displayed indicating the location of the option boards in the card cage of the mainframe. Press the number corresponding to the slot number which the PROM Controller board occupies followed by the RETURN key.

b. Press the [next_test] softkey until the "Supply Adjust" test is highlighted.

c. Press the [disp_test] softkey followed by the [next_test] softkey. Then press the [start] softkey to initializes the "10 volt VP3" test.

d. Measure the voltage at TP6. Adjust R34 for a voltage at TP6 (VP3) between 9.97 and 10.03 volts. Now measure TP5 for 4.65 volts to 5.3 volts.

4-29. The second test "All supplies powered for measurement and adjustment" should now be performed. It is assumed that the "10 volt VP3" test was previously performed and the display is still under the "Supply Adjust" menu. The following is the operating procedure for the "All supplies powered for measurement and adjustment" test:

a. Press the [next_test] softket until the "All supplies are powered for for measurement and adjustment" test is highlighted. Then, press the [start] softkey to stimulate the test.

b. Set up oscilloscope as follows:

CH A: DC....5v/Div. probe to TP6 on 64501A bd. DISPLAY A TRIGGER B

TRIGGER MODE: NORMAL
TRIGGER: POSITIVE SLOPE

*** NOTE ***

All buttons on scope should be in the out position to start. All delay controls must be OFF and all calibrating controls in the detent position.

TIME/DIV .5ms main

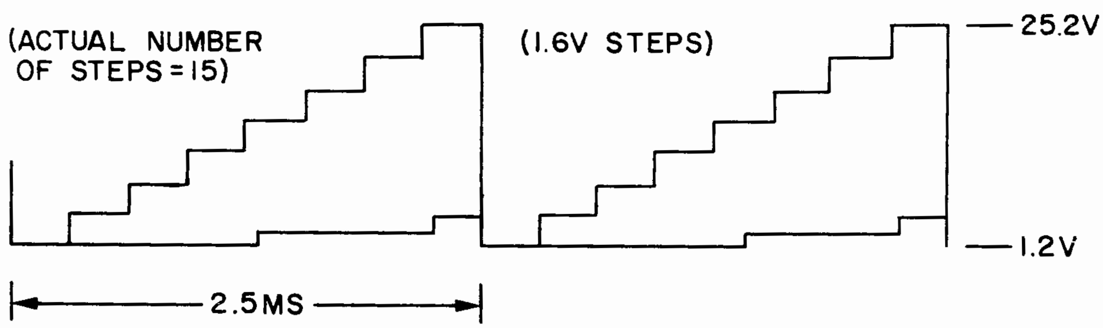


Figure 4-8. VP3 Waveform (1.2v - 26.7v)

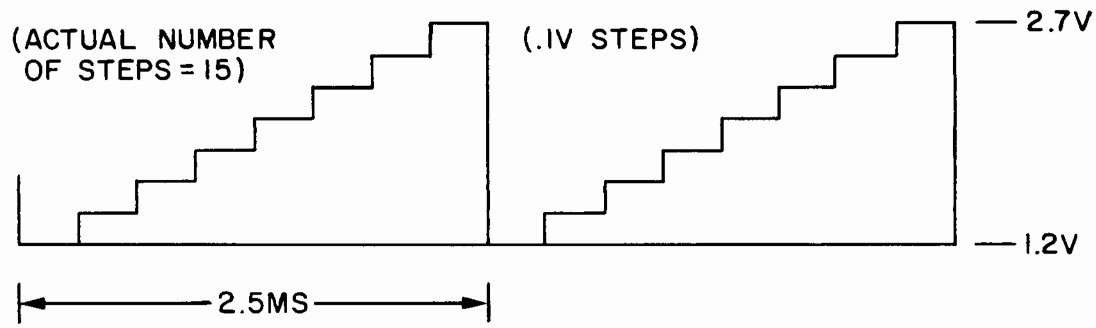


Figure 4-9. VP3 Waveform (1.2v - 2.8v)

e. VP3 is shaped into two ramps. The low end ramp steps from 1.2 to 2.7 volts in equal 0.1 volt increments. This is repeated 10 times. The high end ramp steps from 1.2 to 25.2 volts in equal 1.6 volt increments.

f. Adjust the trigger level for a stable trace. The top part of the waveform should look like figure 4-8. NOTE: The waveform MUST contain 15 steps and be linear.

g. Adjust Channel A for 1v/DIV. The bottom part of the waveform should look like figure 4-9. NOTE: The waveform MUST also contain 15 steps and be linear.

4-30. The "VP3 oveload" test can be tested while running either the "All supplies powered for measurement and adjustment". The "VP3 overload" test can not be directly accessed like the other two tests.

4-31. This test displays both the "# Test" and number of failures. The number of failures (the overload counter) is shown to the left of the "# Test" counter. (See figure 4-7).

4-32. The current overload bit is tested at the last rise of the high end ramp. If the overload bit is detected, the overload counter on the display will be incremented to reflect the overload. The procedure for checking this test is as follows:

a. Place one end of a 50 Ohm 1W resistor into the Prom ZIF socket hole 12 on the 64502A Module. Secure by pushing the ZIF socket insertion lever forward. With either the "All supplies powered for measurement and adjustment" test running, momentarily touch the other resistor lead to the PROM socket hole 21.

CAUTION

The 50 Ohm 1W resistor will get hot! The DAC is capable of approximately 15 watts.

b. The "VP3 overload test" should start counting overloads. This verifies that the overload detector U38 is operating.

Table 4-4. Signature Analysis Loop A

LOOP A - ADDR/ID

MODE = QUAL
CLOCK = pos. edge : U37-2
START = neg. edge : P1-69
STOP = pos. edge : U37-11

Qual = low

Vh = 2A2C

NODE	SIG.	NODE	SIG.	NODE	SIG.
U1-1	2281	U10-19	0000	U16-3	0001
U1-2	3108				
U1-3	346A	U11-1	FC09	U18-1	0000
U1-4	C532	U11-2	FAPA	U18-2	0000
U1-5	1564	U11-3	FA92	U18-13	0000
U1-6	3H71	U11-4	FA8F	U18-14	0000
U1-7	U774	U11-5	5168		
U1-8	F545	U11-6	C240	U19-1	0000
		U11-7	060U	U19-2	0000
U5-3	F2HP	U11-8	0001	U19-14	0000
U5-4	2743				
U5-7	A1H1	U13-3	9710	U22-3	060U
U5-8	PPCC	U13-4	2AAA		
U5-13	7F3F	U13-7	2A0C	U23-1	0000
U5-14	7232	U13-8	2A23	U23-3	0000
U5-17	280P	U13-13	0U53		
U5-18	3P81	U13-14	8C33	U24-1	0000
		U13-17	F426	U24-3	0000
U6-3	7383	U13-18	FF30		
U6-4	060U			U25-1	0000
U6-5	56U2	U14-1	P619	U25-3	0000
U6-6	99PH	U14-2	730F		
U6-7	68PC	U14-3	730F	U26-1	0000
		U14-4	0000	U26-3	0000
U9-11	2A2C	TOTLZ=5			
		U14-5	0000	U27-1	0000
U10-1	2A2C	U14-7	2A2C	U27-3	0000
U10-2	0000	U14-9	5927		
U10-5	0000	U14-10	2A2C	U28-1	0000
U10-6	0000	TOTLZ=1		U28-3	0000
U10-9	0000	U14-11	2A2C		
U10-11	2A2C	U14-12	2A2C	U29-1	0000
U10-12	0000	U14-14	FF32	U29-3	0000
U10-15	0000	U14-15	9515		
U10-16	0000			U30-1	0000

Table 4-4. Signature Analysis Loop A (Cont'd)

NODE	SIG.	NODE	SIG.
U30-3	0000	U39-4	0000
U39-6	2A2C		
U34-2	2A2C	U39-11	0000
U34-3	2A2C		
U34-6	2A2C	U40-6	0000
U35-1	5927		
U35-2	F2HP		
U35-3	3P81		
U35-4	2743		
U35-5	280P		
U35-6	A1H1		
U35-7	7232		
U35-8	PPCC		
U35-9	7F3F		
U36-2	9710		
U36-4	2AAA		
U36-6	2A0C		
U36-8	2A23		
U36-11	0U53		
U36-13	8C33		
U36-15	F426		
U36-17	FF30		
U37-2	0000		
TOTLZ=5			
U37-4	P619		
U37-6	730F		
U37-7	2A2C		
U37-8	730F		
U37-11	0000		
U37-13	2A2C		
U39-3	CU3P		

Table 4-5. Signature Analysis Loop B

LOOP B - DATA

MODE = QUAL
CLOCK = pos. edge : U37-2
START = neg. edge : P1-69
STOP = pos. edge : U37-11

Qual = low

Vh = 5U91

NODE	SIG.
U1-1	0000
U1-2	0000
U1-3	0000
U1-4	0000
U1-5	0000
U1-6	0000
U1-7	0000
U1-8	0000
U5-3	C9AA
U5-4	H2UC
U5-7	P747
U5-8	P271
U5-13	2CH6
U5-14	8CA9
U5-17	CC0C
U5-18	56UF
U6-3	5U91
U6-4	0000
U6-5	5U91
U6-6	5U91
U6-7	5U91
U9-11	5U91
U10-1	5U91
U10-2	0000
U10-5	0000
U10-6	0000
U10-9	0000
U10-11	5U91
U10-12	0000
U10-15	0000
U10-16	0000

NODE	SIG.
U10-19	0000
U11-1	0000
U11-2	0000
U11-3	0000
U11-4	0000
U11-5	0000
U11-6	0000
U11-7	0000
U11-8	0000
U13-3	AUF8
U13-4	5U91
U13-7	5U91
U13-8	5U91
TOTLZ=	
U13-13	5U91
U13-14	5U91
U13-17	5U91
U13-18	5U91
U14-1	UHA8
U14-2	UHA8
U14-3	5498
U14-4	0000
TOTLZ=5	
U14-5	0000
U14-7	0C09
U14-9	5U91
U14-10	5U91
TOTLZ=1	
U14-11	5U91
U14-12	U6A1
U14-14	5U91
U14-15	UHA8

NODE	SIG.
U16-3	0000
U18-1	01PP
U18-2	H1H1
U18-13	6U44
U18-14	19CU
U19-1	AH47
U19-2	98PU
U19-14	C799
U22-3	0000
U23-1	6U44
U23-3	6U44
U24-1	19CU
U24-3	19CU
U25-1	01PP
U25-3	01PP
U26-1	H1H1
U26-3	H1H1
U27-1	C502
U27-3	C502
U28-1	C799
U28-3	AH47
U29-1	AH47
U29-3	AH47
U30-1	98PU

Table 4-5. Signature Analysis Loop B (Cont'd)

NODE	SIG.	NODE	SIG.
U30-3	98PU	U39-3	A239
U39-4	0000		
U34-2	5U91	U39-6	5U91
U34-3	5U91	U39-11	0000
U34-6	5U91		
U40-6	0000		
U35-1	0C09		
U35-2	C9AA		
U35-3	56UF		
U35-4	H2UC		
U35-5	C00C		
U35-6	P747		
U35-7	8CA9		
U35-8	P271		
U35-9	2CH6		
U36-2	AUF8		
U36-4	5U91		
U36-6	5U91		
U36-8	5U91		
TOTLZ=1			
U36-11	5U91		
U36-13	5U91		
U36-15	5U91		
U36-17	5U91		
U37-2	0000		
TOTLZ=5			
U37-4	UHA8		
U37-6	UHA8		
U37-7	5U91		
U37-8	5498		
U37-11	0000		
U37-13	5U91		

Table 4-6. Signature Analysis Loop C

LOOP C - ADDR/ID

MODE = QUAL
CLOCK = pos. edge : U37-2
START = neg. edge : P1-69
STOP = pos. edge : U37-11

Qual = low

Vh= C4C6

NODE	SIG.
U1-1	6H2H
U1-2	6H2H
U1-3	6H2H
U1-4	6H2H
U1-5	6H2H
U1-6	6H2H
U1-7	6H2H
U1-8	6H2H
U5-3	UH95
U5-4	UFA5
U5-7	460H
U5-8	6AA7
U5-13	7847
U5-14	HAPC
U5-17	HUF1
U5-18	HAPC
U6-3	H99C
U6-4	0FC7
U6-5	C8HC
U6-6	C46F
U6-7	H99C
U9-11	C4C6
U10-1	C4C6
U10-2	UF3F
U10-5	UF3F
U10-6	UF3F
U10-9	00HA
U10-11	PP63
U10-12	00HA
U10-15	UF3F
U10-16	00HA

NODE	SIG.
U10-19	UF3F
U11-1	6H2H
U11-2	6H2H
U11-3	6H2H
U11-4	6H2H
U11-5	6H2H
U11-6	6H2H
U11-7	0FC7
U11-8	0000
U13-3	C12F
U13-4	HUF1
U13-7	HUF1
U13-8	HUF1
U13-13	HUF1
U13-14	HUF1
U13-17	68C7
U13-18	773C
U14-1	A8UA
U14-2	UH53
U14-3	A786
U14-4	0000
TOTLZ=5	
U14-5	0000
U14-7	C4C6
U14-9	1330
U14-10	C4C6
TOTLZ=1	
U14-11	C4C6
U14-12	C4C6
U14-14	1F4F
U14-15	55A9

NODE	SIG.
U16-3	0000
U18-1	0000
U18-2	0000
U18-13	0000
U18-14	0000
U19-1	0000
U19-2	0000
U19-14	0000
U22-3	0FC7
U23-1	0000
U23-3	0000
U24-1	0000
U24-3	0000
U25-1	0000
U25-3	0000
U26-1	0000
U26-3	0000
U27-1	0000
U27-3	0000
U28-1	0000
U28-3	0000
U29-1	0000
U29-3	0000
U30-1	0000

Table 4-6. Signature Analysis Loop C (Cont'd)

NODE	SIG.	NODE	SIG.
U30-3	0000	U39-3	P11U
U39-4	0000		
U34-2	C4C6	U39-6	C4C6
U34-3	C4C6	U39-11	0000
U34-6	C4C6		
U40-6	0000		
U35-1	1330		
U35-2	UH95		
U35-3	HAPC		
U35-4	UFA5		
U35-5	HUF1		
U35-6	460H		
U35-7	HAPC		
U35-8	6AA7		
U35-9	7847		
U36-2	C12F		
U36-4	HUF1		
U36-6	HUF1		
U36-8	HUF1		
U36-11	HUF1		
U36-13	HUF1		
U36-15	68C7		
U36-17	773C		
U37-2	0000		
TOTLZ=5			
U37-4	A8UA		
U37-6	UH53		
U37-7	C4C6		
U37-8	A786		
U37-11	0000		
TOTLZ=1			
U37-13	C4C6		

Table 4-7. Signature Analysis Loop D

LOOP D - SOCKET ID

MODE = QUAL
CLOCK = pos. edge : U37-2
START = neg. edge : P1-69
STOP = pos. edge : U37-11

Qual = low

Vh = P672

NODE	SIG.	NODE	SIG.	NODE	SIG.
U1-1	0462	U10-19	0000	U18-1	0000
U1-2	36P3			U18-2	0000
U1-3	CA43	U11-1	399F	U18-13	0000
U1-4	596C	U11-2	399F	U18-14	0000
U1-5	21A1	U11-3	399F		
U1-6	3U93	U11-4	399F	U19-1	0000
U1-7	381U	U11-5	3985	U19-2	0000
U1-8	39UF	U11-6	399C	U19-14	0000
		U11-7	0000		
U5-3	65FF	U11-8	0000	U22-3	0000
U5-4	CF62				
U5-7	A02A	U13-3	7339	U23-1	0000
U5-8	H71P	U13-4	P672	U23-3	0000
U5-13	6367	U13-7	0000		
U5-14	PP77	U13-8	P672	U24-1	0000
U5-17	P472	U13-13	P650	U24-3	0000
U5-18	P6U3	U13-14	P678		
		U13-17	445F	U25-1	0000
U6-3	0P47	U13-18	445F	U25-3	0000
U6-4	0000				
U6-5	8U95	U14-1	A22P	U26-1	0000
U6-6	04C9	U14-2	H117	U26-3	0000
U6-7	1196	U14-3	H117		
		U14-4	0000	U27-1	0000
U9-11	P672	U14-5	0000	U27-3	0000
		U14-7	P672		
U10-1	P672	U14-9	3765	U28-1	0000
U10-2	0000	U14-10	P672	U28-3	0000
U10-5	0000	U14-11	P672		
U10-6	0000	U14-12	P672	U29-1	0000
U10-9	0000	U14-14	445F	U29-3	0000
U10-11	P672	U14-15	7339		
U10-12	0000			U30-1	0000
U10-15	0000	U16-3	0000	U30-3	0000
U10-16	0000				

Table 4-7. Signature Analysis Loop D (Cont'd)

NODE	SIG.	NODE	SIG.
U34-2	P672	U40-6	0000
U34-3	P672		
U34-6	P672		
U35-1	3765		
U35-2	65FF		
U35-3	P6U3		
U35-4	CF62		
U35-5	P472		
U35-6	A02A		
U35-7	PP77		
U35-8	H71P		
U35-9	6367		
U36-2	7339		
U36-4	P672		
U36-6	P672		
U36-8	P672		
U36-11	P650		
U36-13	P678		
U36-15	445F		
U36-17	445F		
U37-2	0000		
U37-4	A22P		
U37-6	H117		
U37-7	P672		
U37-8	H117		
U37-11	0000		
U37-13	P672		
U39-3	954C		
U39-4	0000		
U39-6	P672		
U39-11	0000		

*** MANUAL BACKDATING ***

*** SECTION VIII ***

*** THEORY AND SCHEMATICS ***

8-1. INTRODUCTION.

8-2. This section contains information for troubleshooting and repairing the Model 64501A PROM Programmer.

8-3. The block diagram, schematic, component locator, and other service information are provided on fold-out service sheets to help you in servicing the Model 64501A PROM Programmer. Table 8-1 Logic Symbology will aid you in reading and interpreting the new Logic Symbols.

8-4. BLOCK DIAGRAM THEORY.

8-5. Buffers U35, U36 and U37 are drivers that buffer the Positive PROM Programmer from the CPU Bus.

8-6. Function Selector U14 controls the various functions on the Positive PROM Programmer. U33 determines which direction data will flow through U35.

8-7. U39, U40, and U41 form a Timer to prevent over heating of the Programmer's components if the CPU program fails to operate properly.

8-8. U16 and U22 are used to develop pulses and voltages required to program the PROM.

8-9. U34 developes the board ID of the Positive PROM Programmer Identification Code.

8-10. Socket ID and Current Overload Buffer U9 returns the Programmer Module's Identification Code and Current Overload Status to the CPU.

8-11. DAC Latch U10, DAC U21, Current to Voltage Converter U32, and Adjustable Regulators VR1 and VR2, form a programmable voltage source. The range is +1.2 V to +26.7 V in .1 volt steps.

8-12. U38 is a current overload sensor.

8-13. VR3 and VR4 are Adjustable Voltage Regulators.

8-14. Address Latches U5 and U13 develop the PROM's address.

8-15. Data Write Buffers U23 through U31 write the data to the PROM being programmed.

8-16. Data Read Buffers U18, U19, and U20 return the data read from the PROM to the CPU for verification.

8-17. THEORY OF OPERATION.

8-18. General.

a. The theory of the Positive PROM Programmer is discussed in the order of events as they occur under software control.

b. The Positive PROM Programmer communicates with the CPU over the CPU data bus. Only two address lines are used, LA12 and LA13.

c. The addresses for the PROM being programmed are developed on the Positive PROM Programmer P.C. board.

d. U35 buffers the lower eight bits of the CPU data bus. Control lines LWRT, LSEL, and LSTB from the CPU in conjunction with U33 determine if U35 is in the send or receive mode.

e. U36 buffers the upper eight bits of the CPU data bus, and is receive only on the Positive PROM Programmer.

f. U37 buffers CPU control lines LSTB, LWRT, LA12, LA13, LSEL LPOP.

g. Function Selector U14 decodes LA12, LA13, and LWRT to control data flow on the Positive PROM Programmer.

8-19. DETAILED THEORY.

8-20. Fail Safe Timer.

8-21. U39, 40, and U41 form a "Failsafe Timer" that uses the output of U41 as the clock. Normally the timer is reset by the software at least every 100 milliseconds. If the program fails to execute properly or some other failure occurs, the timer will not be reset and will count all 32 states (approx 500 milliseconds). This forces U39 pin 8 low, clearing the Address Latches U5 and U13, DAC Latch U10, and Data Write Latch U31.

8-22. Pulse Generators.

8-23. U16 and U22 are dual positive AND drivers. There are two sections of each IC which are connected in parallel to provide 500 milliamps of current sinking ability. The two signals developed by the CPU (LD14,15) are used to generate pulses and voltage levels of different values. The different values can be found in the theory of operation for each of the programmer modules.

8-24. Positive PROM Programmer Identification.

8-25. When the CPU forces LIDEN, LSEL, and LSTB low, and the Positive PROM Programmer is present in the mainframe, a low state on LD12 is developed by board ID U34. (Pull-up resistors on the CPU data bus pull other data lines high.) EFFF HEX is returned to the CPU on the data bus. If FFFF HEX is returned, the CPU will not allow Positive PROM Programming.

8-26. Programmer Module Identification.

8-27. Programmer module identification code is developed on the module's P.C. board. The ID code is generated by grounding combinations of lines ID0 through ID4, A12, and A13 in the programmer module. A12 and A13 are shared between PROM address and ID code. R1 and R2 allow the programmer module to pull A12 and A13 low for the ID code without damaging the outputs of Address Latch U13, even if they are high.

8-28. The ID code is buffered by ID and Current Overload Buffer U9, and is returned through U35 when requested by the CPU. The CPU uses the ID code to determine which PROMs may be programmed in the module installed in the mainframe. The unique code for each module may be found in the theory of operation for the programmer modules.

8-29. Programmable Positive Power Supply.

8-30. After the PROM is installed, the CPU programs power supply VP3 and checks the power being used by the PROM. The DAC Latch U10 latches digital information from the CPU for the Digital-to-Analog Converter, U21. DAC U21 is referenced to +5 V supplied by an adjustable regulator, VR1. DAC U21 converts the 8 bit digital word to a programmed current level that drives the Voltage to Current Converter U32.

8-31. U32 is a current to voltage converter referenced to +29 V. Depending on the current from the the DAC U21 the output voltage will range from approximately 0 V to +25.5 V. With the 8 bit resolution of U21, the output of U32 will have a resolution of .1 V.

8-32. Adjustable Regulator VR2 is referenced to +40 V allowing the output to "follow" the Voltage to Current Converter U32. VR2's output is always +1.2 V greater than U32's output. Therefore, the output of VR2 will vary from +1.2 V to +26.7 V in .1 V steps (U21's input: 00 HEX=+1.2 V, FF HEX=+26.7 V). R23 and R24 share power dissipation with VR2.

8-33. Current Sensor.

8-34. R20 and R21 are current sensing resistors that develop a voltage proportional to the current being drawn by the PROM. R18 and R19 are load resistors for VR2 when there is no PROM in the module's socket.

8-35. Current Source Q1 develops 20 millivolt across R17 with 1 milliamp of current. R17's 20 millivolt in addition to the voltage developd across R20 and R21, with no load, will keep U38's output in the high state. This indicates to the CPU that less than 400 milliamps is being drawn from VR2.

8-36. When current through R20 and R21 is greater than 400 milliamps, the voltage accross R20 and R21 becomes great enough to offset the 20 millivolts accross R17. When this happens, the output of U38 goes to a low state indicating to the CPU that an overload condition exists. The CPU then programs the Power Supply to +1.2 V until the overload is removed.

SECTION VIII

THEORY AND SCHEMATICS

8-1. INTRODUCTION.

8-2. This section contains information for troubleshooting and repairing the Model 64501A PROM Programmer.

8-3. The block diagram, schematic, component locator, and other service information are provided on fold-out service sheets to help you in servicing the Model 64501A PROM Programmer. Table 8-1 Logic Symbology will aid you in reading and interpreting the new Logic Symbols.

8-4. BLOCK DIAGRAM THEORY.

8-5. POSITIVE PROM PROGRAMMING (not operation). During the programming sequence, information is burned into the PROM and then "read". The "read" is a dummy read and nothing is verified. The actual read/verify occurs after the PROM has been completely programmed. After the PROM is programmed, the information in the PROM is read and compared to the information in the user file. Consult specific PROM Programmer Module Service Manual for further details.

8-6. The sequence of events are different for the various PROMs and will not be presented in detail here. For detailed information see the appropriate manufacturer's data sheets on the PROM being programmed.

8-7. U3A and U3B latch the address to the PROM being programmed. The address is clocked into the flip-flops by U7C when directed by the CPU. They will be cleared in the event of any power-up sequence by LPOP, or by the Failsafe Timer.

8-8. U6B latches the data to be written to the PROM being programmed. The data is clocked into the flip-flops by U7C when directed by the CPU. They will be cleared in the event of any power-up sequence by LPOP, or by the Failsafe Timer.

8-9. Data Write Buffers U4A thru U4D, and U5A thru U5D are dual positive AND drivers. Each section of the drivers can sink about 250 milliamps. Both sections are connected in parallel to allow sinking of 500 milliamps. The PROM data write lines are connected in different ways for each programmer module, and are discussed in detail in the theory-of-operation for each module.

8-10. PROM DATA VERIFICATION. Verification is done through Data Read Buffers U3D and U3F. U3D and U3F provide a high impedance input for the PROM. U3D and U3F are made TTL compatible by R8 and R9, setting the input threshold to +1.2 volts. Resistor Package RP4 pulls the comparators up for the inputs of the Data Read Buffers U6C.

8-11. When requested by the CPU, through Function Selector U7C (LDR), the data will be returned to the CPU for verification via U6C and U6A.

8-12. Signals in the PROM Programmer have been assigned Mnemonics that describe the active state and function of the signal line. Mnemonic functional definitions are listed alphabetically in Table 8-2.

8-13. THEORY OF OPERATION.

8-14. General.

8-15. Buffers U6A, U6D and U7B are drivers that buffer the Positive PROM Programmer from the CPU Bus.

8-16. Function Selector U7C controls the various functions on the Positive PROM Programmer. U6D, U7D, and U7E determine which direction data flows through U6A.

8-17. U8C, and U8D form a Timer to prevent over heating of the Programmer's components if the CPU program fails to operate properly.

8-18. U4E and U5E are used to develop pulses and voltages required to program the PROM.

8-19. U6E, U7D, and U7E develop the board ID of the Positive PROM Programmer Identification Code as well as signature analysis and data direction control.

8-20. Socket ID and Current Overload Buffer U3C returns the Programmer Module's Identification Code and Current Overload Status to the CPU.

8-21. DAC Latch U8A, DAC U7A, Current to Voltage Converter U6G, and Adjustable Regulators VR1 and VR2, form a programmable voltage source. The range is +1.2 to +26.7 volts in .1 volt steps.

8-22. U6F is a current overload sensor.

8-23. VR3 and VR4 are adjustable voltage regulators.

8-24. Address Latches U3A and U3B, develop the PROM's address.

8-25. Data Write Buffers U4A thru U4D, U5A thru U5D and Write Latch U6B write the data to the PROM being programmed.

8-26. Data Read Buffers U3D, U3F, and U6C return the data read from the PROM to the CPU for verification.

8-27. The theory of the Positive PROM Programmer is discussed in the order of events as they occur under software control.

8-28. The Positive PROM Programmer communicates with the CPU over the CPU data bus. Only two address lines are used, LA12 and LA13.

8-29. The addresses for the PROM being programmed are developed on the Positive PROM Programmer PC board.

8-30. U6A buffers the lower eight bits of the CPU data bus. Control lines LWRT, LSEL, and LSTB from the CPU in conjunction with U6E, U7D determine if U6A is in the send or receive mode.

8-31. U7B buffers the upper eight bits of the CPU data bus, and is receive only on the Positive PROM Programmer.

8-32. U6D buffers CPU control lines LSTB, LWRT, LA12, LA13, LSEL LPOP.

8-33. Function Selector U7C decodes LA12, LA13, LWRT, LSEL, and LSTB (which are derived thru U7E) to control data flow on the Positive Prom Programmer

8-34. DETAILED THEORY.

8-35. FAILSAFE TIMER. U8C, and U8D form a "Failsafe Timer" that uses the output of U8C as the clock. Normally the timer is reset by the software at least every 100 milliseconds. If the program fails to execute properly or some other failure occurs, the timer will not be reset and will count all 32 states (approx approximately 500 milliseconds). This forces U8B pin 6 low, clearing the Address Latches U3A and U3B, DAC Latch U8A, and Data Write Latch U6B. It also lowers VP1 and VP2 to 1.2 volt, and grounds the +5, -5, +12, -12 volt sources to the pod.

8-36. COLD SOCKET. At all times except during Prom Module Identification and Program/Read Cycles, the Prom Module is kept in a Cold Socket state which leaves all the output lines to the Prom Module in a grounded state. Cold Socket can be triggered from any one of three sources: 1) Failsafe timer, 2) LPOP, and 3) Software.

8-37. POSITIVE PROM PROGRAMMER IDENTIFICATION. At the slot where the Prom Programmer Control board resides, a low signal is forced on the mainframe data bus LD12 by U6E when the CPU forces LID, LSEL, and LSTB low. Pull-up resistors on the mainframe data bus pull all the other data lines to a high state. U6A is disabled and U7B is in an input mode so they do not interfere on the data bus. The code generated and returned to the CPU is EFFF Hex (1000 Hex low true).

8-38. PULSE GENERATORS. U4E and U5E are dual positive AND drivers. There are two sections to each IC which are connected in parallel to provide 500 milliamps of current sinking ability. The two signals developed by the CPU (LD14, 15) are used to generate pulses and voltage levels of different values on the programmer module.

8-39. PROGRAMMER MODULE IDENTIFICATION. The Prom Module Identification Code is developed on the module's PC board. The ID code is generated by grounding combinations of lines ID0 through ID4, A12, and A13 in the Prom module. A12 and A13 are shared between PROM address and ID code, but can only be used as ID or Address in any ONE application. R4 and R5 allow the PROM Module to pull A12 and A13 low for the ID code without damaging the outputs of Address Latch U13, even if they are high.

8-40. The ID code is buffered by ID and Current Overload Buffer U3C, and is returned through U6A when requested by the CPU. The CPU uses the ID code to determine which PROMs may be programmed in the module installed in the mainframe. The unique code for each module may be found in the theory-of-operation for the Prom Programmer Modules.

8-41. MOTHERBOARD POWER SUPPLIES. The Prom Programmer Control board uses the +12, -12, +5, -5, and +40 volt supplies from the Motherboard. The +5 volt supply is only used for the Prom Control board circuitry and is not used on the Prom modules. The Prom Control board takes the +12 volt supply and regulates (LM317T) it to generate the +5 volt reference that is used on the Prom modules and as a reference voltage by the Digital-to-Analog Converter (DAC).

8-42. The +5 volt reference can be adjusted by changing the voltage on the adjust line of the voltage regulator VR1. A 50 Ohm potentiometer R34 in series between the adjust line and ground allows adjustment of the +5 volt reference between 4.65 volts to 5.3 volts.

8-43. The +12, +5 reference, -5, and -12 volt supplies are sent to the Prom Module through gating circuitry. The High Voltage Supply used on the Control Board is generated by a +40 volt supply from the the Motherboard.

8-44. CONTROL BOARD VOLTAGES SUPPLIED TO PROM MODULE. The Prom module has available to it four fixed voltage supplies, two hardware programmable supplies and one software programmable supply.

8-45. The +12 and -12 will supply 500 milliamps of current with less than a 2% voltage drop from the supply line and 300 milliamps with less than a 1% drop from the supply voltage. The +5 and -5 supplies will each source 800 milliamps current with no more than a 2% voltage drop from the supply line.

8-46. The two hardware programmable supplies are controlled by a voltage generated on the Prom module. The voltage range is from 1.2 volts to 37 volts. The software programmable supply is set under software control and has a voltage range of 1.2 to 26.7 volts in 0.1 volt increments.

8-47. Supply Voltage Gating. Two control lines L HOT SOCKET and L COLD SOCKET are generated on the Prom Control board to either turn ON or turn OFF the supply voltages to the Prom module. The control signals are mutually exclusive.

8-48. +5 Volt Gating. The +5 volt supply is gated by use of two paralled p-channel FETs 6I, 7I, and one open collector gate U7G. When the supply is gated to the Prom module, the FETs look like a series resistance of no greater than 0.15 Ohms in the supply line. When the supply is gated OFF for Cold Socket, the line has a low impedence (348 Ohm) path to ground through the open collector gate.

8-49. -5 Volt Gating. The -5 volt supply is gated with two parallel n-channel FETs 8I, 9I and one p-channel FET 8H. When the supply is gated to the Prom module, the n-channel FETs look like a series resistance of no greater than 0.15 Ohms in the supply line. When the supply is gated OFF for Cold Socket, the line has a low impedence (348 Ohm) path to ground through the p-channel FET.

8-50. +12 Volt Gating. The +12 volt supply is gated by a single p-channel FET 9H and one high voltage open collector gate U8F. When the supply is gated to the Prom module, the FETs look like a series resistance of no greater than 0.6 Ohms in the supply line. When the supply is gated OFF for Cold Socket, the line has a low impedence (1K Ohm) path to ground through the open-collector gate.

8-51. -12 Volt Gating. The -12 volt supply is gated by a p-channel FET 6H and a n-channel FET 7H. When the supply is gated to the Prom module, the FETs look like a series resistance of no greater than 0.6 Ohms in the supply line. When the supply is gated off for Cold Socket, the line has a low impedence (1K Ohm) path to ground through the n-channel FET.

8-52. VP3. VP3 refers to the Bus Latch U8A, Digital-to-Analog Converter U7A, Op amp U6G, and Adjustable Voltage Regulator VR2. The bus latch simply provides a constant digital input to the digital-to-analog converter.

8-53. Since there are 8 bits of binary data presented to the converter, there are 256 different values for the current that the converter can assume. Each step adds approximately 7.8 microamps of current to the initial value starting at 0 amps ranging to a maximum value of 2.00 milliamps.

8-54. The Op amp acts as a current-to-voltage converter. The current generated by the digital-to-analog converter is drawn through the 12.71K Ohm resistor R29 and therefore produces a voltage swing of roughly 0 to 25.5 volts in 0.1 volt increments.

8-55. The adjustable regulator uses the voltage provided by the Op amp as the reference voltage for the the output stage of the regulator. The output is always 1.2 volts above the adjust voltage level. Therefore, VP3 is capable of providing a regulated voltage of 1.2 to 26.7 volts in 0.1 volt increments.

8-56. VP3 Limitations. The input to the voltage regulator is 40 volts through 25 Ohms. The regulator must have at least a 3 volt drop across it in order to stay in regulation and therefore, the worst case condition is the output at 26.7 volts and the input at 30 volts. For the input to drop from 40 to 30 volts, the current through the 25 Ohm resistor would have to be 400 milliamps. Any current requirements of greater than 400 milliamps cannot be supplied at 26.7 volts. The LM317 can supply more current than 400 milliamps, but only at voltage levels less than 26.7 volts.

Table 8-1. Logic Symbology

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

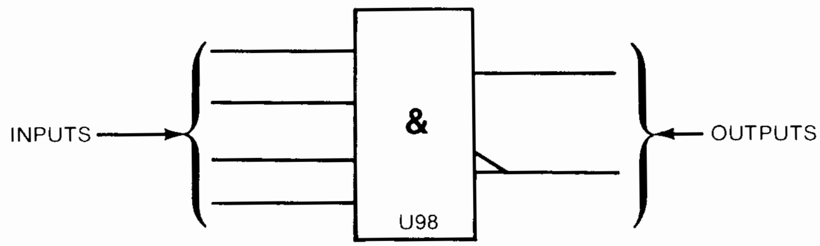
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

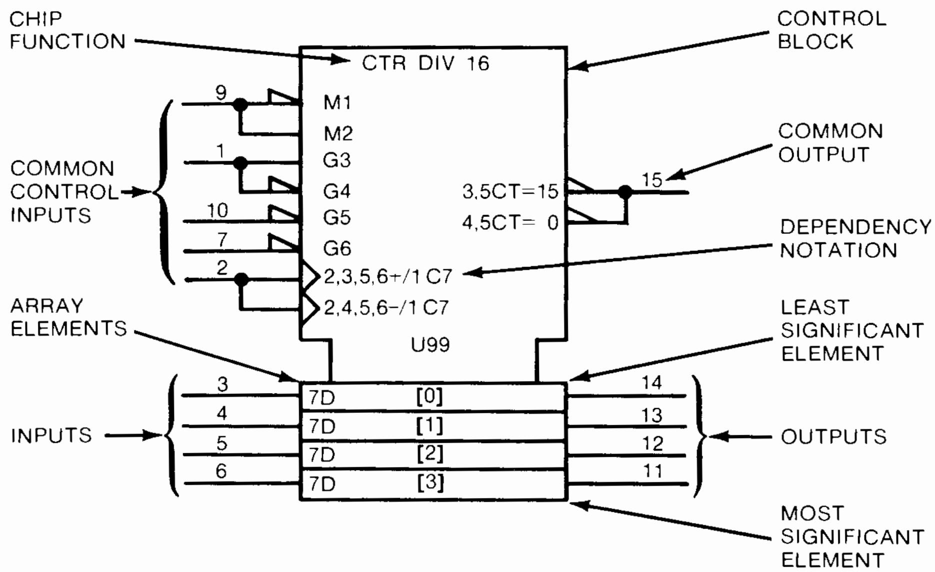
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in [ ]).

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Table 8-1. Logic Symbology

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (complements state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-1. Logic Symbology

OTHER SYMBOLS

∩	Analog Signal
&	AND
} {	Bit Grouping
▷	Buffer
!	Compare
▷	Dynamic
=1	Exclusive OR
⎍	Hysteresis
?	Interrogation
—	Internal Connection
⊾ ⊿	Inversion
O	Negation
—✳—	Nonlogic Input/Output
◇	Open Circuit (external resistor)
◇	Open Circuit (external resistor)
≥1	OR
◇	Passive Pull Down (internal resistor)
◇	Passive Pull Up (internal resistor)
⌝	Postponed
←	Shift Left (or up)
→	Shift Right (or down)
/	Solidus (allows an input or output to have more than one function)
▽	Three State
,	Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
( )	Used for factoring terms using algebraic techniques.
[ ]	Information not defined.
Φ	Logic symbol not defined due to complexity.

LABELS

BG	Borrow Generate
BI	Borrow Input
BO	Borrow Output
BP	Borrow Propagate
CG	Carry Generate
CI	Carry Input
CO	Carry Output
CP	Carry Propagate
CT	Content
D	Data Input
E	Extension (input or output)
F	Function
J	J Input
K	K Input
P	Operand
T	Transition
+	Count Up
−	Count Down

MATH FUNCTIONS

Σ	Adder
ALU	Arithmetic Logic Unit
COMP	Comparator
DIV	Divide By
=	Equal To
>	Greater Than
<	Less Than
CPG	Look Ahead Carry Generator
π	Multiplier
P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal
BIN	Binary
BUF	Buffer
CTR	Counter
DEC	Decimal
DIR	Directional
DMUX	Demultiplexer
FF	Flip-Flop
MUX	Multiplexer
OCT	Octal
RAM	Random Access Memory
RCVR	Line Receiver
ROM	Read Only Memory
SEG	Segment
SRG	Shift Register

DELAY and MULTIVIBRATORS

⎍⎍	Astable
⊢100 ns⊣	Delay
1⎍	Nonretriggerable Monostable
NV	Nonvolatile
I	State of initial power up
⎍	Retriggerable Monostable

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Table 8-2. PROM Programmer Mnemonics

Mnemonic	Description
A0-15	Address 0 through 15 -- these sixteen address signals are sent to the Programmer Module from the PROM Programmer. Some or all of them may be used to program a PROM. They are derived from the data sent to the PROM Programmer over the CPU Data Bus (LD0-15) by the CPU.
DR0-7	Data Read 0 through 7 -- these data signals are used to read the contents of a programmed PROM. The data read is sent to the CPU over the CPU Data Bus for verification. Some or all of these signals may be used.
DW0-7	Data Write 0 through 7 -- these data signals are used to write to the PROM being programmed. The data sent to the PROM is derived from the information sent over the CPU Data Bus by the CPU. Some or all of these lines may be used.
LID0-4	Low Identification 0 through 4 -- these five signals are used to return Identification Codes from the Programmer Modules to the CPU over the CPU Data Bus. By returning an ID Code,the CPU can determine which Programmer Module is installed, and therefore, can tell the operator via the CRT which PROMs may be programmed.
LA12-13	Low Address 12 and 13 -- two of sixteen address signals from the Address Bus (P/O CPU Bus) used to select different functions on the PROM Programmer.
LADD	Low Address -- when low, allows the information on the CPU Data Bus to be latched into the Address Latches. From the outputs of these two latches, the information becomes the address for the PROM being programmed.
LD0-15	Low Data 0 through 15 -- a 16 bit bidirectional bus that is part of the CPU Bus.
LDAC	Low Digital to Analog Converter -- when low, allows the CPU's Data Bus information to be latched into the DAC Latch, setting the voltage at TP3 (VP3).
LDR	Low Data Read -- when low, allows the data read from the programmed PROM to be returned to the CPU for verification.
LDW	Low Data Write -- when low, allows the CPU's Data Bus information to be latched into the Data Write Latch. The outputs of the Latch become the Data to be written to the PROM being programmed.

Table 8-2. PROM Programmer Mnemonics (Cont'd)

Mnemonic	Description
LID	Low Identification -- when low, allows the Identification Code from the Programmer Module to be buffered by the ID and Current Sense Buffer, and returned to the CPU over the CPU's Data Bus. Current Overload Status is also sent to the CPU at this time.
LIDEN	Low Identification Enable -- when low along with LSEL, and LSTB, LD12 will go low. When LD12 is low and the other Data Lines are high, the CPU will recognize that there is a Positive PROM Programmer installed in the Mainframe's Card Cage.
LP1-2	Low Program 1 and 2 -- these two lines are used in conjunction with VP1 and VP2 to develop the various voltages and waveforms used to program PROMs. Sometimes LP1 and/or LP2 are looped back from the Programmer Module to VP1 and/or VP2.
LPOP	Low Power On Pulse -- resets all latches on the PROM Control Board, so that power dissipation is minimal. LPOP will override the Timer in the event of an AC Power transient. When low, causes LRST to go low.
LRST	Low Reset -- when low, LRST will reset both Address Latches, the Data Write Latch, and the DAC Latch. Resetting these Latches causes the Address to be 0000 HEX with 00 HEX being the Data written, and the lowest power dissipation possible in the PROM being programmed.
LSEL	Low Select -- when low, enables the CPU to interact with the Prom Programmer. The CPU can write to (LWRT low), read (LWRT high), or read ID (LIDEN low) from the Prom Programmer.
LSTB	Low Strobe -- when LSTB and LWRT are both low, the CPU is writing to a device over the CPU's Data Bus. If LSEL is also low, the PROM Programmer will receive the information. If LSEL is high, the PROM Programmer will not pay attention to the information sent on the bus. If LSTB is low, and LWRT is high, and the PROM Programmer is selected (LSEL low), then the PROM Programmer will return information to the CPU over the CPU's Data Bus.
LTRST	Low Timer Reset -- Resets the failsafe timer when low.
LWRT	Low Write -- when low, indicates the CPU is writing to the addressed device.

Table 8-2. PROM Programmer Mnemonics (Cont'd)

Mnemonic	Description
VP1-2	Voltage, Programmable 1 and 2 -- Adjustable Regulators used for developing various voltages and waveforms used for programming PROMs. The adjustable inputs (VP1R and VP2R) can be connected to LP1 and LP2 or to voltage dividers located on the Programmer Modules.
VP1R, VP2R	Voltage, Programmable Regulated -- Inputs to VR3 and VR4 which program their outputs to +1.2 volts above VP1R and VP2R respectively.
VP3	Voltage, Programmable 3 -- Output of voltage regulator VR2 used for developing various voltage levels used for programming PROMs. VP3 is under program control due to DAC U7A.

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Monjitas 454 of. 206
SANTIAGO
Tel: 395752, 398296
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A

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Tel: 225-5044
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13 Community Center
New Friends Colony
NEW DELHI 110 065
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Computation and Measurement
Systems (CMS) Ltd.
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C,CM,E,P

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